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INSTRUCTION MANUAL
FOR THE
PCM DATA PROCESSOR
OF THE
SATELLITE TELEMETRY AUTOMATIC REDUCTION SYSTEM (STARS)

GODDARD SPACE FLIGHT CENTER

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INSTRUCTION MANUAL

For The

PCM DATA PROCESSOR

of the

SATELLITE TELEMETRY
AUTOMATIC REDUCTION SYSTEM
(STARS)

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ADDENDUM TO THE STARS PCM DATA PROCESSOR MANUAL

PCM DATA PROCESSOR SPECIFICATIONS

Input Data Code	:	NRZ, Split Phase
Input Data Bit Rate	:	250,000 Bits/Second (Maximum)
Word Sync	:	Up to 3 bits
Frame Sync Word	:	Up to 32 bits
Data Word	:	Up to 32 bits
Data Frame	:	Up to 128 words
Subcommutation	:	Synchronous and Asynchronous
Synchronous Subcom*	:	Up to 128 frames
Asynchronous Subcom*	:	a) Up to 3 subcoms, each subcom having a sync word of up to 32 bits. b) One subcom with up to 128 words, and two subcoms with up to 64 words.
Output Data **	:	Thirty-two data and 5 flag lines
Output Commands***	:	Time Present (sync) Data Present (sync) Alternate Data Present (sync) Subcom Sync Dump Auxiliary Command
Input Power	:	115 $\pm$10v ac, 60 cps at 30A

* Synchronous and asynchronous subcoms as referred to herein are, respectively, those which have the same word or words in every frame and are distinguished from each other by means of a unique and common number of words (or counts); and those which may have independent sync codes, or identical sync codes and arbitrarily assigned frame words anywhere within the main frame.

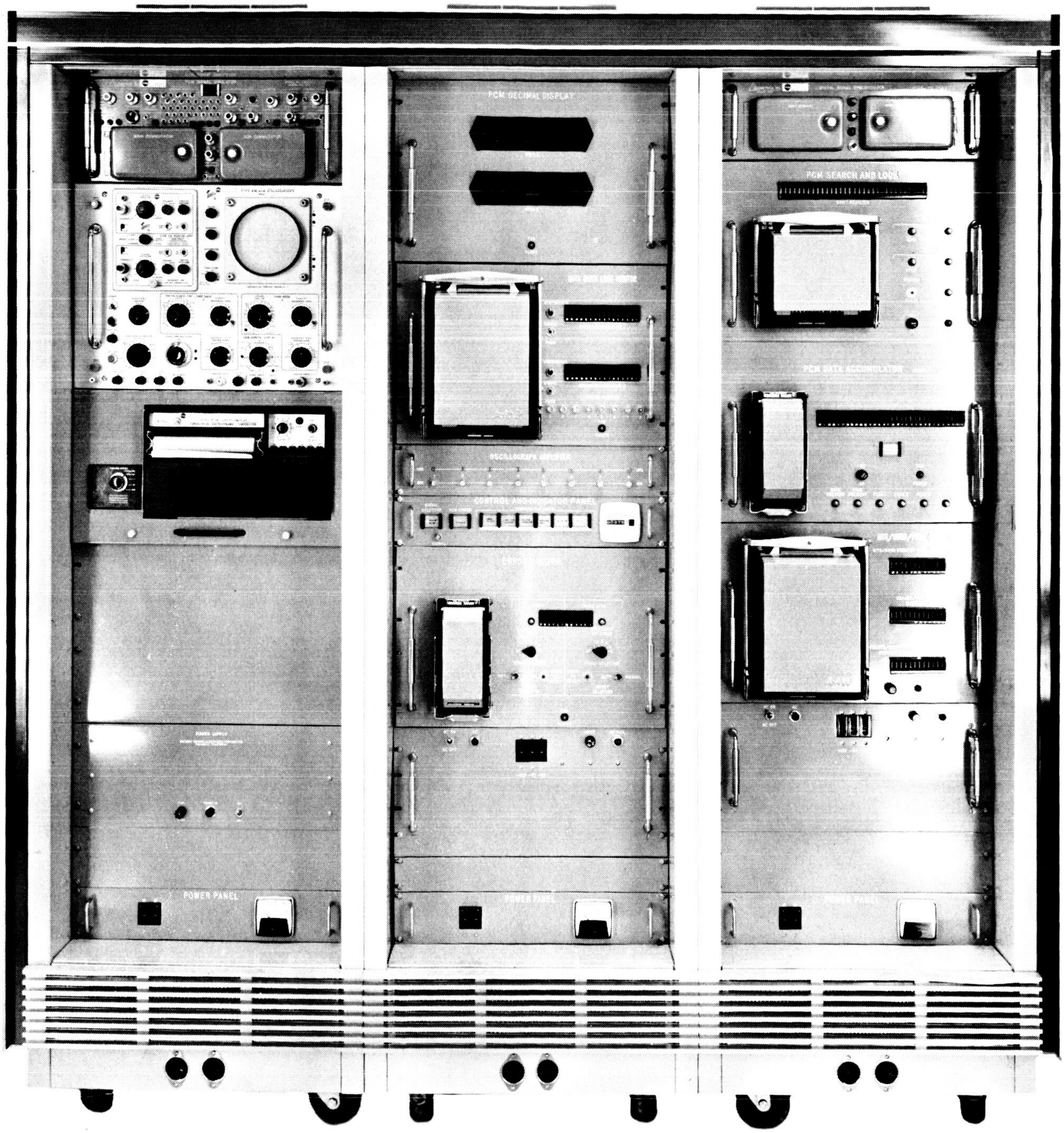
** Negative level (-6v dc) represents binary "1" and ground (0v dc) represents binary "0".

*** Positive, 2-3 μs pulses, from -6v dc to ground.

LOCATION OF CIRCUIT BOARDS DESCRIBED IN FIGURES OF THIS MANUAL

The following list relates the appropriate figure (or figures) to the Unit and S-Block wherein the illustrated circuit boards are located.

Figure	Unit	S-Block
III-2	Search & Lock	III
III-3	"	II
III-4	"	III
III-5	"	I
III-6	"	III
III-7	"	II
III-8	"	I
III-9	B/W/F Counters	I
III-10	"	I
III-11	"	III
III-12	"	III
III-13	"	III
III-14	"	II
III-15	"	II
III-16	"	II
III-17	"	I
III-18	Accumulator	I
III-19	"	I
III-20	"	I
III-21	"	II
III-22	Error Monitor	I
III-23	"	I & III
III-24	"	II
III-25	Quick Look	II
III-26	"	II
III-27	"	II
III-28	"	I
III-29	Decimal Display	III
III-30	"	II
III-31	"	III
III-32	"	I



Frontispiece. PCM Data Processor of the Satellite Telemetry Automatic Reduction System (STARS)

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ILLUSTRATIONS

ILLUSTRATIONS (Cont'd)

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SECTION I

GENERAL DESCRIPTION OF SYSTEM

A. PURPOSE

This manual describes the function, installation and operation, and theory of operation of the STARS (Satellite Telemetry Automatic Reduction System) PCM Data Processor. The Data Processor is part of the STARS PCM Data Processing line, which includes the Time Decoder, Buffer, Analog and Digital Tape Transports.

The manual consists of six sections:

(1) General Description

(2) Installation and Operation

(3) Theory of Operation

(4) Patch Panel Programming

(5) Special Circuits

(6) Power Distribution and Wiring

The information contained in this manual is detailed to the component board (logic unit) level and should assist in maintaining as well as operating the equipment. Illustrations are provided to augment the description of the equipment. Illustrations pertaining to a section will be found at the end of that section. They are identified by a prefix number indicating the section and the actual figure number: e.g., III-5, meaning Section III, figure 5.

Since each section is independent, the table of contents is compiled by section.

B. PCM CODES

PCM TELEMETRY

Definition of PCM

The spacecraft data which is reduced by the Data Processor is a pulse code modulated (PCM) serial train of binary bits representing digital and analog measurements. The serial train of pulses (bits) is divided into equal groups of N bits each called "words." The presence or absence of each of the N bits describes the level of the sample of the analog quantity to the nearest discrete step between zero and full scale. In other words, each analog measurement made aboard the satellite is digitized with the same sampling rate and number of bits representing full scale.

The digitized quantity may be encoded for transmission in one of several codes as shown in figure I-1. Waveform no. 2 is NRZ-change which maintains one level for "1" bits and a different level for "0" bits. In waveform no. 3 there is a transition (positive or negative) for every "1" bit and no transition for "0" bits. Waveform no. 4 is the split-phase or bi-phase code, where a "1" bit is identified by a "downward" transition and a "0" bit is identified by an "upward" transition, hence bi-phase. This code is used predominantly in GSFC's spacecraft. The fifth waveform is a "return-to-zero level" code such that there is a pulse for every "1" bit and no pulse for zero bits. This code is seldom used.

PCM Data

The actual PCM signal as received from the spacecraft, recorded by the station, and reproduced by the Data Processor tape recorders may be noisy, distorted, and degraded. To reconstruct its waveform the signal is fed to the Bit Synchronizer unit where it is filtered, bit synchronized, and reconditioned for use by the Data Processor's Search and Lock Unit. The Bit Synchronizer is capable of handling any of the codes shown in figure I-1.

The Data Processor normally uses the bi-phase data. However, at times, when the bi-phase signal from the tape recorder is degraded considerably, the Bit Synchronizer may be operated in the NRZ-C mode at twice the nominal bit rate in order to minimize bit phase reversal. This is possible because bi-phase is equivalent to sampling NRZ-C twice per bit period (see fig. I-1, waveform 2 and 4). When this mode is used, the clock signal supplied by the Bit Synchronizer to the Search and Lock unit must be divided by 2 so that in the Data Processor the NRZ-C signal and the clock signal are maintained at the same bit rate.

The clock and data signals are 90 degrees out of phase with respect to each other. This is done in order to sample the incoming data bits at 90 degrees or 270 degrees of the bit period; thus the bi-phase data is always treated as NRZ-C by the Search and Lock unit (see figure III-2).

A detail description of PCM telemetry is given in "Aerospace Telemetry", Ch. 6, Harry L. Stiltz Editor, published by Prentice Hall.

C. FUNCTIONAL DESCRIPTION OF SYSTEM

FUNCTIONAL DESCRIPTION OF THE STARS PCM DATA PROCESSOR

Purpose

The STARS PCM Data Processor described in this manual is part of the Satellite Telemetry Automatic Reduction System designed to reduce "analog" pulse code modulated (PCM) data received from the satellite into a format acceptable by an IBM, Univac 1107, or equivalent computer for complete decommutation and generation of experimenter's tapes. The Data Processor is the "front end" of STARS which includes the Time Decoder and Buffer.

The purpose of the Data Processor is: (a) to present to the buffer the serial train of telemetry data in terms of digital words of proper length and location in the main frame, (b) supply the required commands to the buffer to sample the presented data in proper order, as well as sample time presented by the Time Decoder, (c) generate special buffer commands to properly begin and terminate data blocks, (d) check the frame sync code and bit errors, and flag the status thereof, and (e) generate special flags, such as subcom word(s) location, signal mode, etc., to minimize the effort required in decommutating and further processing of experimenter's data.

General

The Data Processor is designed to accept any PCM telemetry format using split phase or NRZ coding. It meets the specifications outlined in GSFC's Aerospace Data Systems Standards, January 1963, Section 1. Figure I-2 is the complete block diagram of the Data Processor. As shown in this figure, the Processor consists of the following units: Search and Lock, Bits/Word/Frame Counters, Accumulator, Decimal Display, Quick Look, Error Monitor, and Bit Synchronizer and Signal Conditioner. A multitrace oscilloscope and strip chart recorder are provided to monitor the incoming and outgoing signals. A digital data simulator is included to enable performance of quick operational checks and to aid in maintaining the equipment.

Data recorded on tape, in serial binary code, is supplied by various NASA tracking stations. These tapes, known as "analog tapes," are played back on CEC's VR-2600 tape recorders which are part of the STAR System. Since telemetry formats differ with different satellites, the Data Processor is programmed by means of patch panels to accommodate any known format of a particular satellite. Programming includes selection of word length, frame length, permissible frame sync bit errors, subcom frame length, number of frames to acquire frame sync, number of frames to flywheel, number of bad frames after which to revert to search mode, and setting up the frame and subcom frame sync recognizers for particular frame sync codes. In addition, patching is used to program the generation of buffer command signals in accordance with the desired buffer tape format and buffer requirements to produce buffer tapes.

Functions

The basic buffer commands generated by the Data Processor are: Time Present, Data Present, Alternate Data Present, Subcom Sync, Dump, and Frame Sync Quality. These commands in conjunction with the data available on parallel lines, enable the Computer Format Control Buffer to generate "digital" tapes of a prescribed computer format for each satellite.

Data synchronization and generation of buffer commands is accomplished by the following units: Bit Synchronizer, Search and Lock, B/W/F Counters and Accumulator. Specifically, telemetry data from the analog tape is bit synchronized and conditioned (determination of ones and zeros) in the Bit Synchronizer unit. Frame synchronization takes place in the Search and Lock unit in conjunction with the B/W/F Counters and Accumulator units. Subcom frame synchronization is accomplished in the B/W/F Counters unit. Data in parallel form is supplied to the buffer from the Accumulator where all buffer commands are generated.

Monitoring of certain data words is done in the Quick Look unit. The Decimal Display unit converts binary words into decimal equivalents and displays them. Parity errors and frame sync bit errors are detected, counted and displayed in the Error Monitor Unit.

The purpose of and the functions performed by the Data Processor have been described above. The detail description of the theory of operation of the equipment, how the various functions are generated in each unit, is described in Section III.

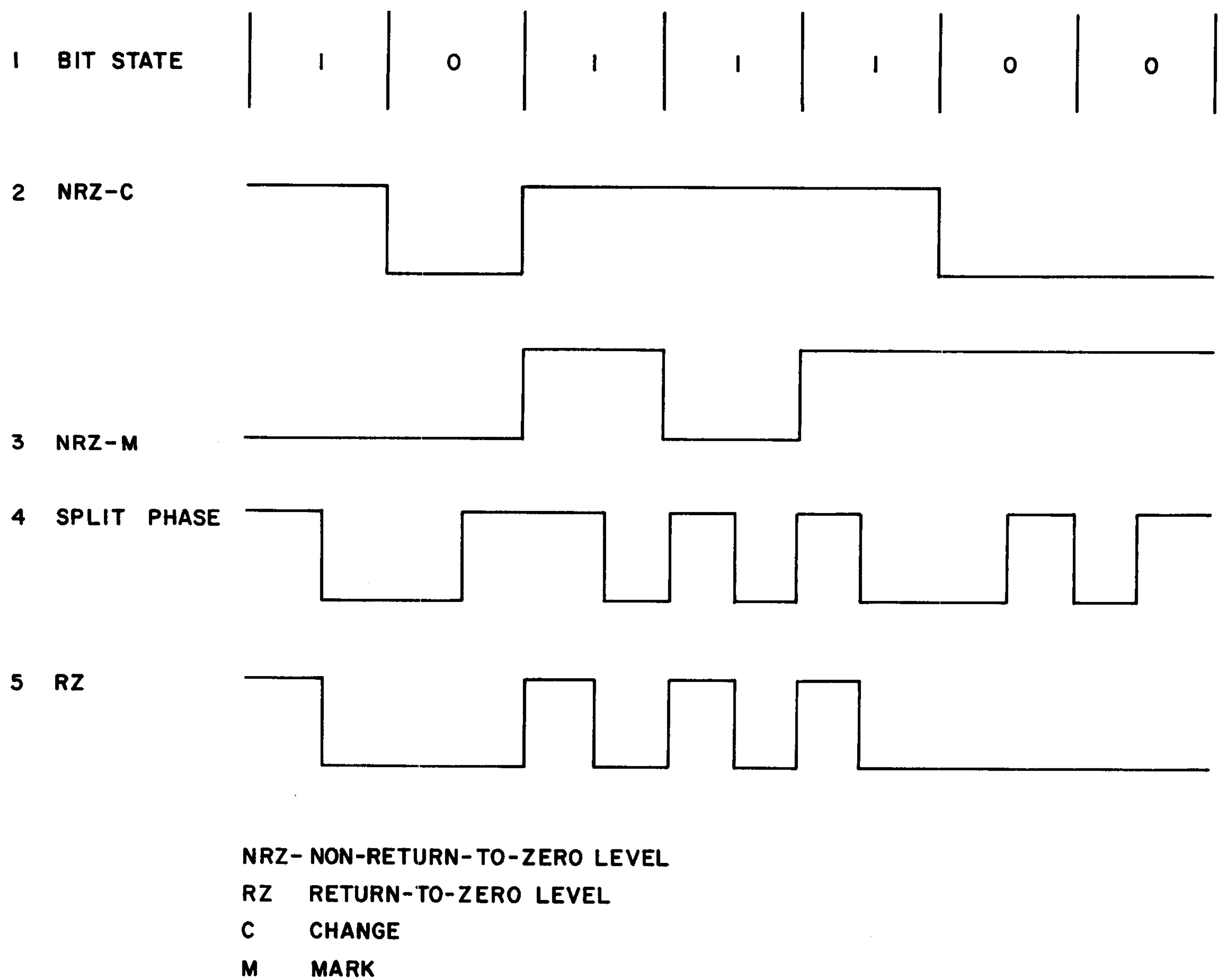


Figure I-1. PCM Coding

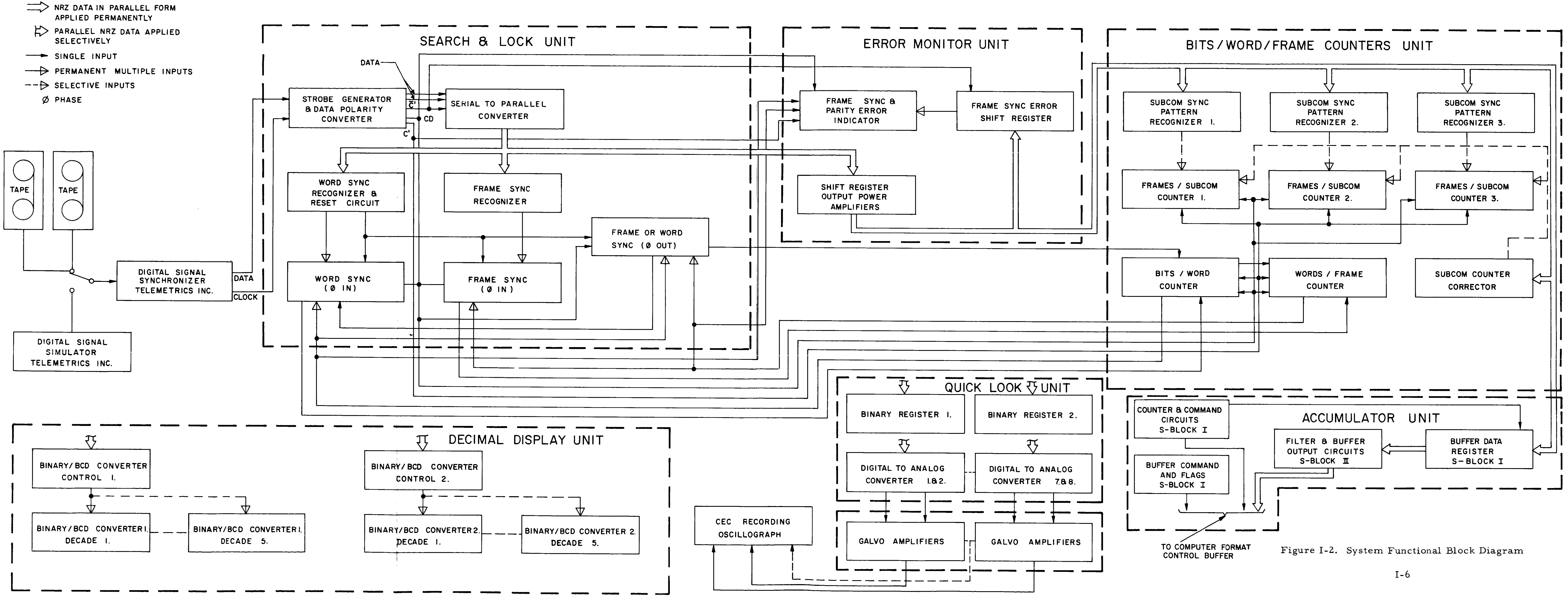


Figure I-2. System Functional Block Diagram

SECTION II

INSTALLATION AND OPERATION

A. INSTALLATION

The on-line units of the STARS PCM Data Processor system are contained in relay racks A, B, and C (left to right) as shown in the frontispiece. Interunit cabling is supplied with the rack.

B. CONTROLS AND INDICATORS

A brief functional description of the controls, indicators, and connectors associated with each unit of the STARS PCM Data Processor is provided in Tables II-1 through II-13.

Table II-1. Control and Indicator Panel, Controls and Indicators (Figure II-1)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
1	SIGNAL SELECTOR switch TAPE SIM	A 2-position push button switch. Selects input signal source to signal synchronizer. Switch plate glows green when tape is selected, red when simulated input signal is selected.
2	PCM POWER switch POWER	A 2-position push button switch. Controls application of ac power to racks A, B, and C. Switch plate glows green when power is applied.
3	TEMPERATURE LIMITS DEC. DISP. QUICK LOOK DATA ACCUM ERROR MON W-B-F S-L	Indicator lights provide visual overtemperature alarm signals. Individual translucent panels glow red when operating temperature of associated units exceeds 55° C. One each for decimal display, data quick look monitor, PCM data accumulator, error monitor, bits/word/frame counter, and PCM search and lock units, respectively, as marked.
4	HOURS meter	Records elapsed time, while ac power is applied by PCM POWER switch, in hours and tenths of hours. Provides continuous visual display in Arabic numerals.
5	SIGNAL jack	Front panel coaxial connector used to monitor input signal selected.

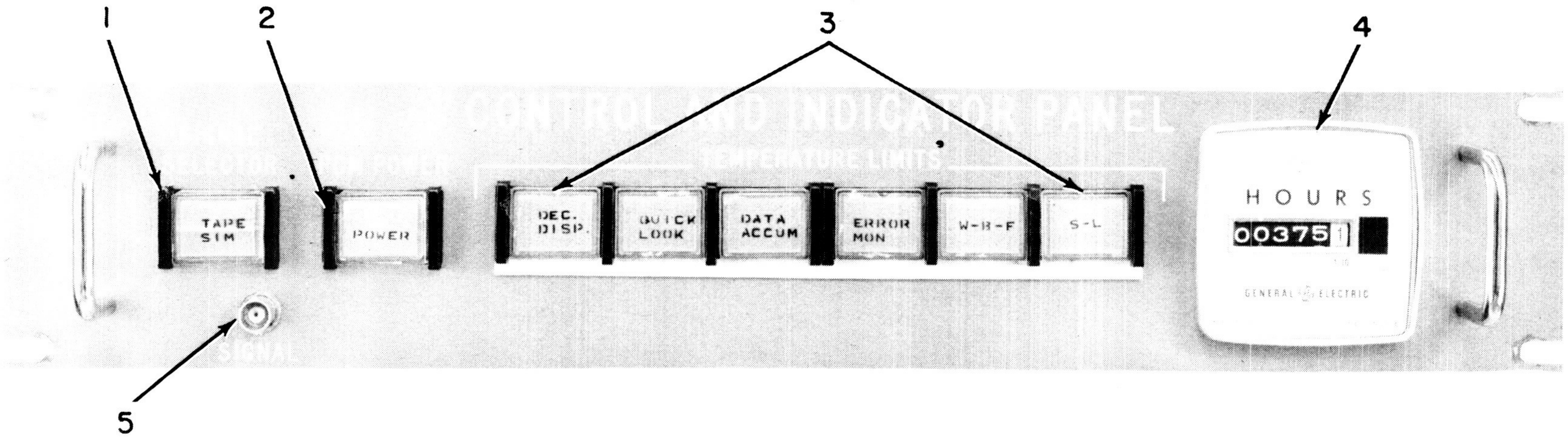


Figure II-1. Control and Indicator Panel, Controls and Indicators

Table II-2. Power Panels, Controls and Indicators (Figure II-2)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
1	ON/OFF switch	15 amp ac circuit breaker, typical of three panels. Dual toggle (ganged) action, provides independent manual on-off control of primary power to racks A, B, and C for all associated system units and convenience outlets. Delayed magnetic overload breaker action automatically protects circuits of each rack.
2	AC VOLTS	Panel mounted rms voltmeter, typical of three panels. Indicates presence and amplitude of applied primary power individually for racks A, B, and C.

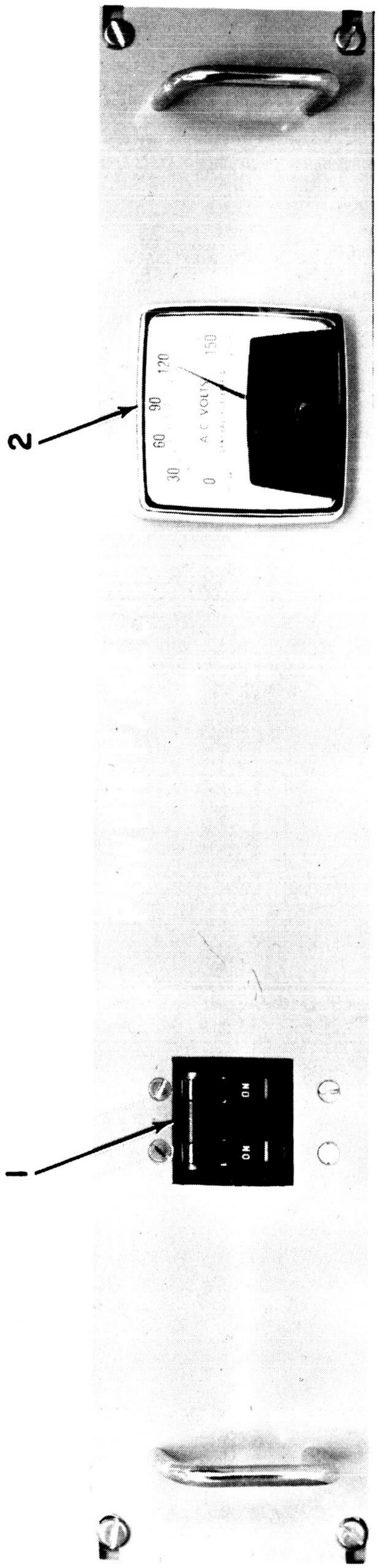


Figure II-2. Power Panels, Controls and Indicators

Table II-3. Power Supplies, Controls and Indicators (Figures II-3 and II-4)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
	Rack A; Dressen-Barnes Power Supply (Figure II-3)	
1	Fuse and Holder	Non-indicating type holder contains a 1 amp glass cartridge fuse in series with primary power switch.
2	Indicator Light	Incandescent lamp with green jewel. Glows when primary power is applied, if continuity exists through fuse.
3	ON/OFF switch	Toggle switch controls application of primary power to the power supply.
	Racks B and C: Computer Control Company Power Supply, Model RP-32 (Figure II-4)	All controls and indicators typical of both racks.
1	AC ON/AC OFF switch (S1)	SPDT toggle action manually controls application of primary power to unit.
2	AC indicator light (DS1)	Incandescent lamp with green jewel. Glows when primary power is applied and continuity through F1 exists.
3	+12v ON/OFF (CB1) - 6v ON/OFF (CB2) -18v ON/OFF (CB3)	Individual toggle type circuit breakers: CB1, 2 amps; CB2 and CB3, 22 amps each. Provide individual manual, and automatic overload control of, application of + 12v, -6v and -18v secondard power outputs, respectively.

Table II-3. Power Supplies, Controls and Indicators (Cont'd)
(Figures II-3 and II-4)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
4	INPUT fuse (F1)	Amp slo-blow glass cartridge fuse and holder, in series with primary power.
5	DC FAIL indicator light (DS2)	Incandescent lamp with red jewel. Glows when +12v, -6v, or -18v secondary power output is interrupted, provided S1 is in AC ON position, and DS1 is energized.
	recessed front panel adjustments (R8, R35, R56)	Secondary power output level adjustments for +12v, -6v, and -18v, respectively (left to right, facing panel). These controls are potentiometers with shafts slotted to accommodate screwdriver blade. Range of adjustment is 2% in each case. NOTE Field adjustment for recalibration not recommended. If necessary, meter used should be accurate to ±0. 5% of full scale indication.

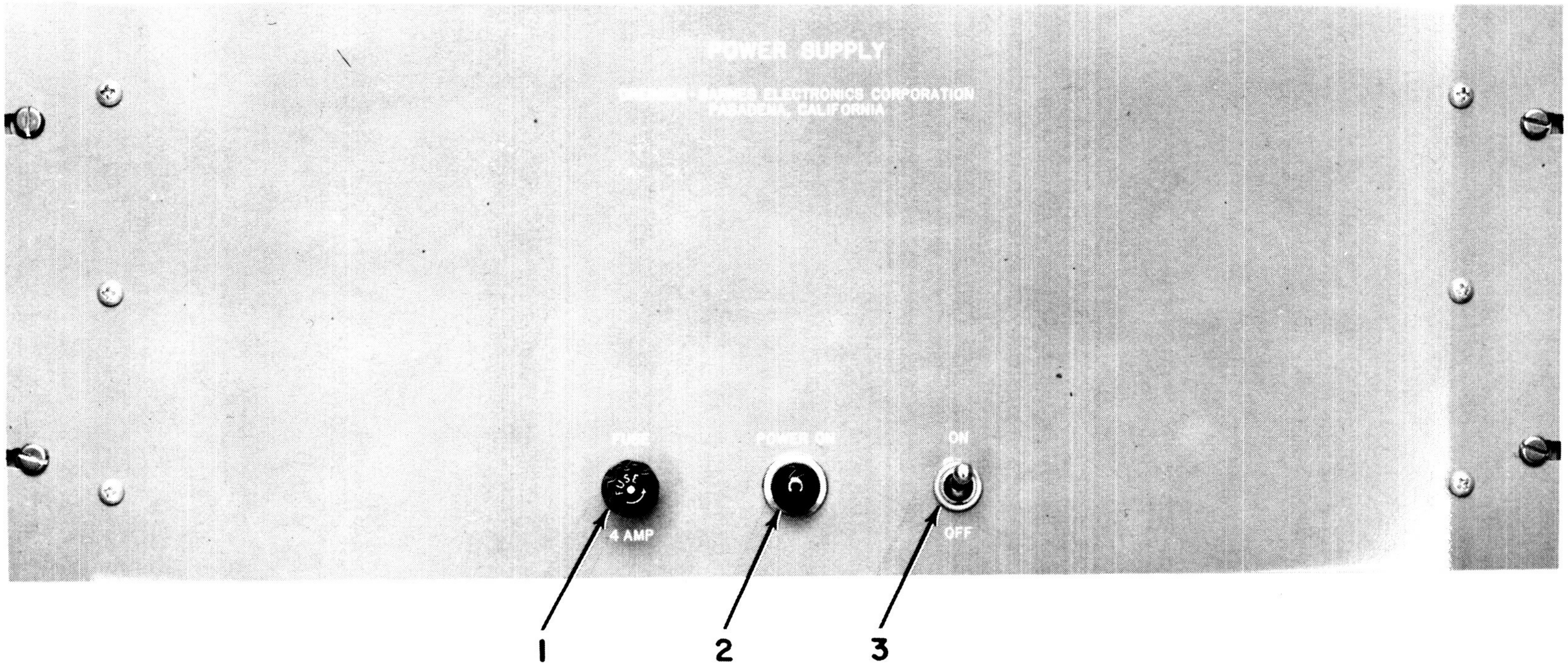


Figure II-3. Dressen-Barnes Power Supply, Controls and Indicators

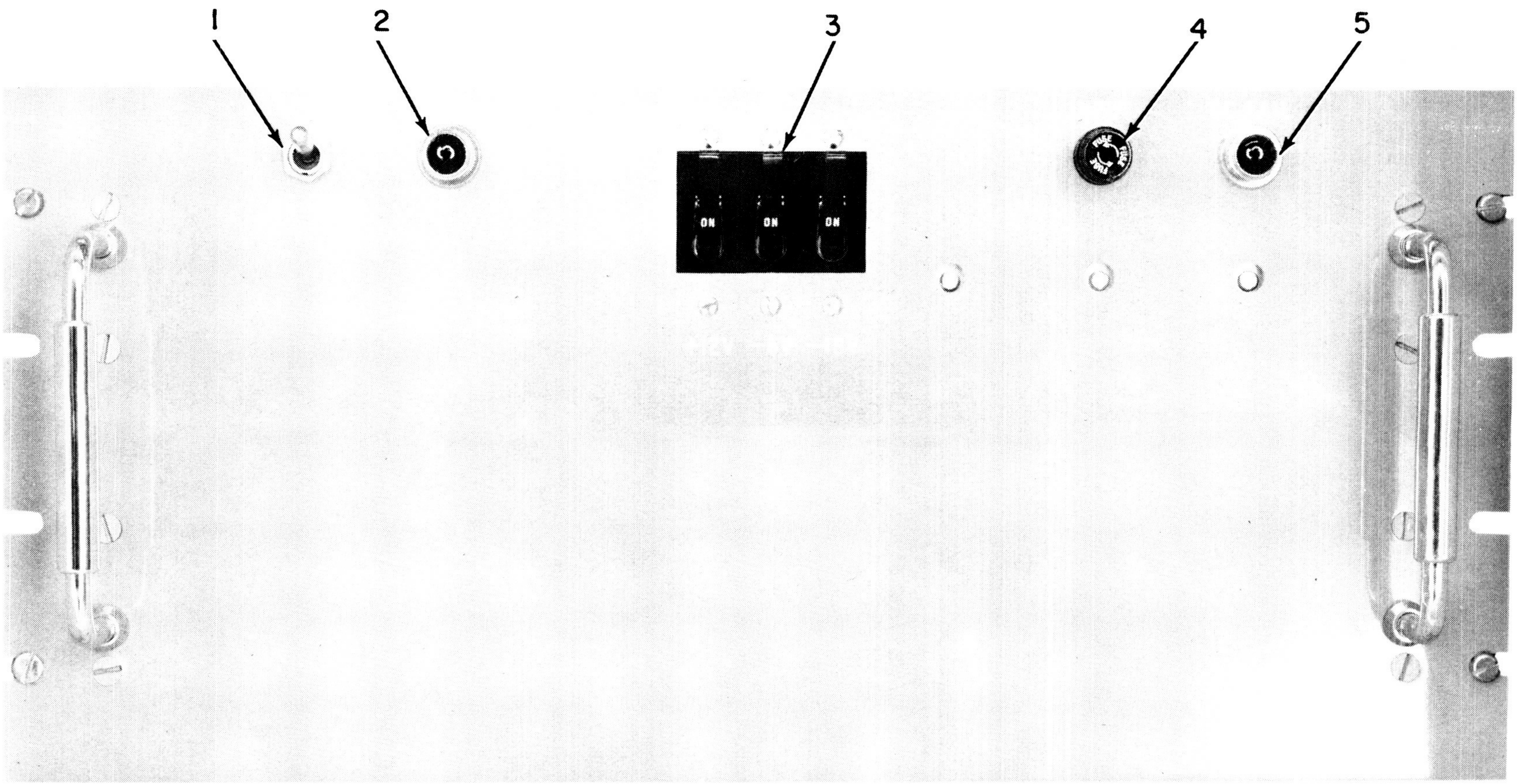


Figure II-4. RP-32 Power Supply, Controls and Indicators

Table II-4. Digital Signal Synchronizer, Controls and Indicators (Figures II-5 and II-6)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
1	Selector Switch	
	REC OR SIMULATOR section	This section of the selector switch prepares the unit for one of three types of single-channel inputs from either a receiver, simulator or tape. These input signals may be positive, negative, or balanced (signal equally above and below a reference voltage).
	TAPE section	This section of the selector switch prepares the unit for one of four types of dual-channel tape inputs. The tape input is dual track and may be dual positive (++), the first track positive and the second negative (+-); the first track negative and the second positive (-+), or dual negative (--).
2	Selector Switch	Selects RZ, NRZ, NRZ space, or bi-phase as the type of signal input to the unit.
3	CHANNEL A	
	INPUT jack	Permits monitoring input data applied to channel A.
4	AMP OUT jack	Permits monitoring data output of first two d-c amplifiers located in channel A
5	DET IN jack	Permits monitoring output of third d-c amplifier which is the data input to level detector (voltage decision circuit) located in channel A.

Table II-4. Digital Signal Synchronizer, Controls and Indicators (Cont'd) (Figures II-5 and II-6)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
6	FREQUENCY SELECTION K.C. selector switch	Permits selecting frequency ranges for internal oscillator between 3 pps and 800K pps. (±20%)
7	OSCILLATOR	
	FINE control	Allows fine adjustment of internal oscillator frequency.
8	HIGH/LOW switch	Allows coarse adjustment of internal oscillator frequency within range selected at FREQUENCY SELECTION K.C. switch.
9	VCO/XTAL toggle switch	Selects either the internal voltage controlled oscillator (VCO) or crystal for generating internal clock rate.
10	VCO CAL	
	SERVO toggle switch	OPEN position opens servo control loop used in setting VCO frequency the CLOSED position closes the servo loop.
11	PUSH TO CALIBRATE pushbutton	Pressing this pushbutton resets the internal up-down counter to cause the nominal center control voltage to be supplied to the VCO.
12	LOOP BANDWIDTH selector switch	Permits selection of servo loop bandwidth.
13	VCO CONTROL meter	Used when calibrating and adjusting the internal voltage controlled oscillator (VCO). Meter indicates analog correction voltage applied to VCO.

Table II-4. Digital Signal Synchronizer, Controls and Indicators (Cont'd) (Figures II-5 and II-6)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
14	CHANNEL A	
	DET OUT jack	Permits monitoring data output from level detector in channel A.
15	LEVEL jack	Permits monitoring d-c level at level detector in channel A.
16	DATA SAMPLE INVERSION	Operative only when NRZ or bi-phase inputs are being accepted. Determines sample polarity. In the "up" position, data will be sampled at -12 V. In the "down" position, data will be sampled at 0 V. Changing switch positions will invert the data output of the Synchronizer.
17	Selector Switch	Selects one of three signal sources for input to unit; receiver, simulator, or tape.
18	GAIN control	Attentuates input signal.
19	FREQ SELECT rotary switch	Set at lowest frequency by keeping the setting at 190-380 always.
20	FINE ADJUST potentiometer	Set in center and remains at this setting.
21	KC FREQ SELECTOR rotary switch	Set to the bit rate of the telemetry data signal.
22	Detector Level Adjust potentiometer (located in Card DET 213)	Adjusts the level such that it is centered on the detector input waveform.

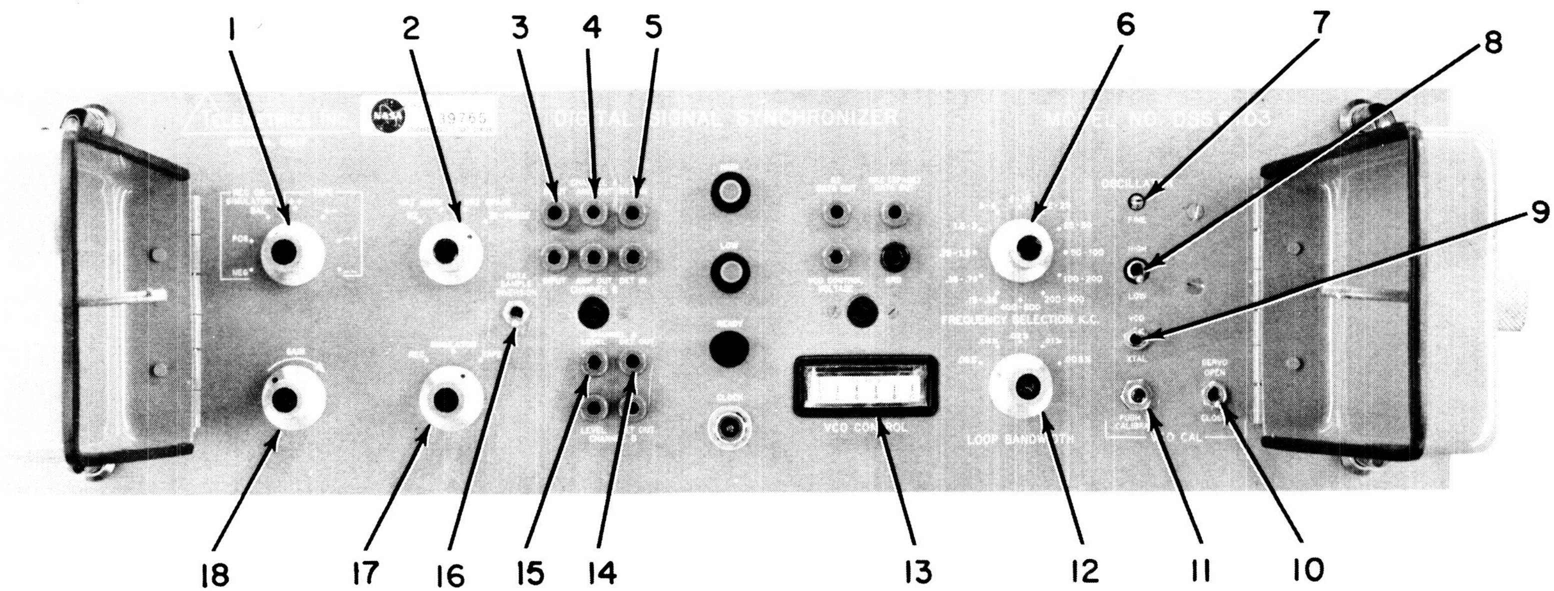


Figure II-5. Digital Signal Synchronizer, Front View, Controls and Indicators

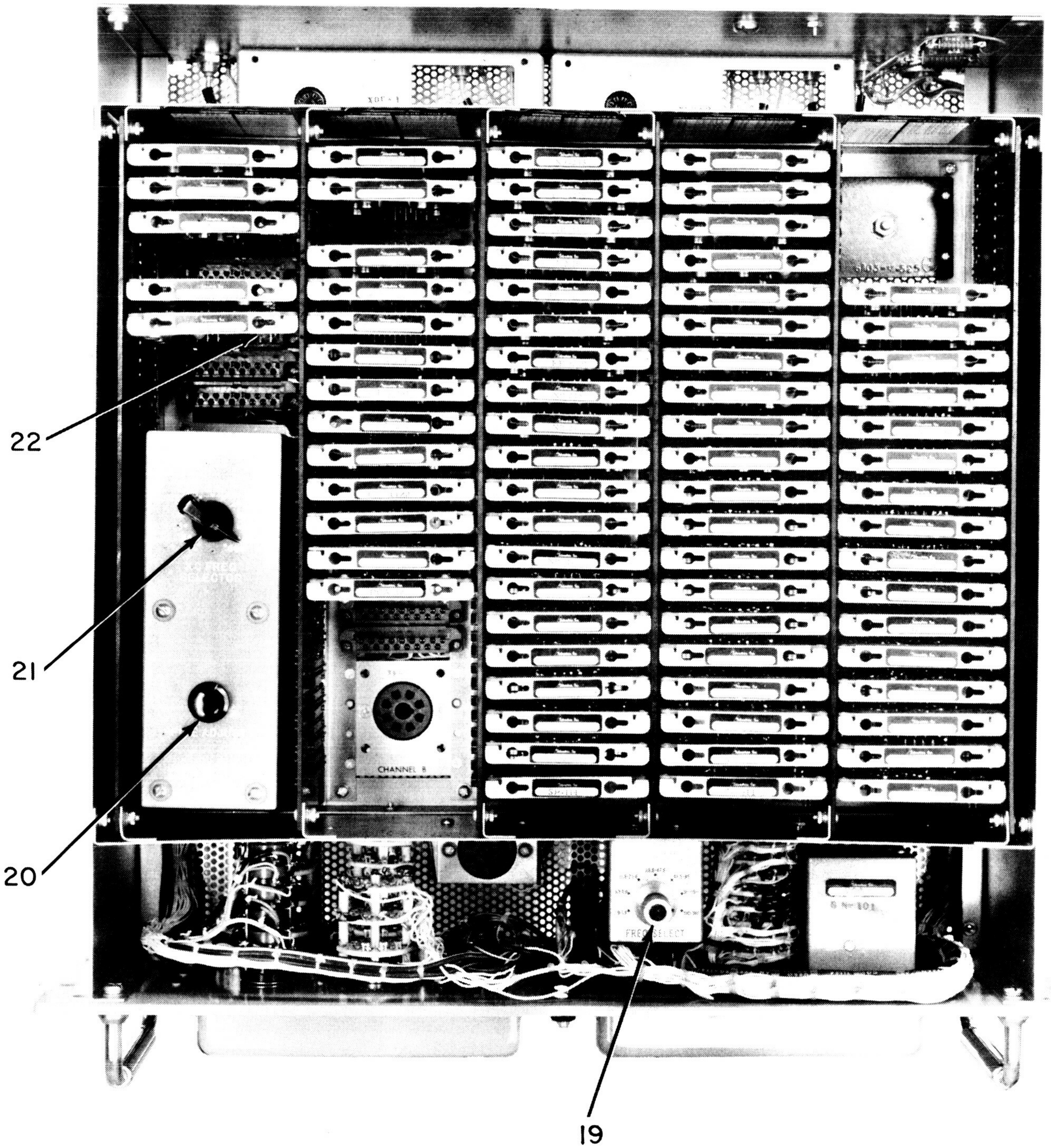


Figure II-6. Digital Signal Synchronizer, Top View, Controls and Indicators

Table II-5. PCM Search and Lock, Controls and Indicators (Figure II-7)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
1	Patchboard	Used to program the PCM search and lock unit. Desired internal interconnections are patched by using jumpers between appropriate patchboard holes (see programming section). Flywheel timing pulses, word sync code, frame sync code, and sync acquisition time are controlled by programming the patchboard.
2	SHIFT REGISTER indicator lights	Assembly of 32 Amperex indicator triodes, each of which indicates the digital status of one stage of the data output shift register. Each lighted indicator signifies presence of a binary one; extinguished indicators signify presence of binary zeroes.
3	WORD indicator lights: LOCK SEARCH	Operating status of unit is indicated by light which is energized. When word sync is lost, SEARCH light is energized; otherwise LOCK light is energized, indicating word sync has been acquired.
4	FRAME indicator lights: LOCK SEARCH	These lights function same way as WORD lights, with respect to acquisition, or loss of frame sync.
5	SUBFRAME COUNTER INCORRECT indicator light	When energized, indicates that subframe counter of B/W/F counters unit is not in sync with subframe counter in satellite.
6	SYSTEM RESET pushbutton	Provides manual control of operating status. When pressed, sync counters are reset and search mode is initiated.

Table II-5. PCM Search and Lock, Controls and Indicators (Cont'd) (Figure II-7)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
7	FAN POWER indicator light	Incandescent lamp with amber jewel. Glows when power is applied to fan motors of unit.
8	-6v, .5A fuse	1/2 amp fuse in series with -6 vdc secondary power from RP-32 power supply.

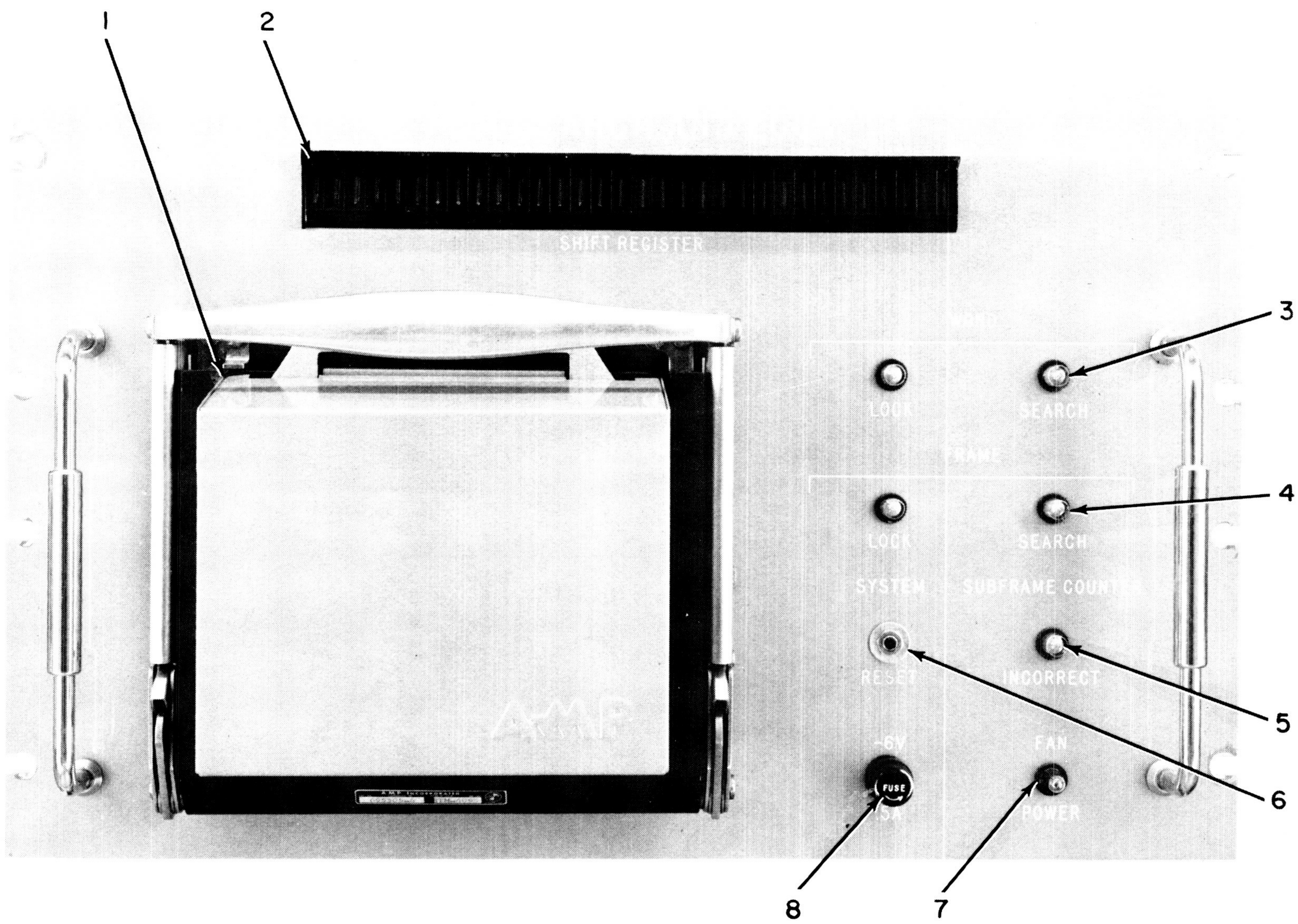


Figure II-7. PCM Search and Lock, Controls and Indicators

Table II-6. PCM Data Accumulator, Controls and Indicators (Figure II-8)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
1	Patchboard	Used to program flow of data from accumulator to buffer. Data present pulse, time present pulse, and flag pulses are controlled by using jumper wires between appropriate holes of patchboard (see programming section).
2	Indicator Light Assembly: 1 through 32	Group of individual Amperex indicator triodes which indicate status of each stage of output shift register as visual binary display. Each lighted indicator represents a binary one and extinguished indicators represent binary zeroes. Indicators 1 through 18 and 23 through 27 are coupled directly to shift register. Indicators 19, 20, 21 and 22 may be coupled through patchboard to shift register or to auxiliary flag generators. Indicators 28 through 32 are coupled to auxiliary flag generators.
3	Selector Switch: DATA PRESENT DATA DELETE	DPDT illuminated switch plate with push-to-change action. Enables or inhibits data flow to buffer. Glows green in DATA PRESENT position and data is presented to buffer. Glows red in DATA DELETE position and data flow stops.
4	-6v, .5A	1/2 amp fuse, in series with -6 vdc secondary power from RP-32 power supply.

Table II-6. PCM Data Accumulator, Controls and Indicators (Figure II-8)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
1	Patchboard	Used to program flow of data from accumulator to buffer. Data present pulse, time present pulse, and flag pulses are controlled by using jumper wires between appropriate holes of patchboard (see programming section).
2	Indicator Light Assembly: 1 through 32	Group of individual Amperex indicator triodes which indicate status of each stage of output shift register as visual binary display. Each lighted indicator represents a binary one and extinguished indicators represent binary zeroes. Indicators 1 through 18 and 23 through 27 are coupled directly to shift register. Indicators 19, 20, 21 and 22 may be coupled through patchboard to shift register or to auxiliary flag generators. Indicators 28 through 32 are coupled to auxiliary flag generators.
3	Selector Switch: DATA PRESENT DATA DELETE	DPDT illuminated switch plate with push-to-change action. Enables or inhibits data flow to buffer. Glows green in DATA PRESENT position and data is presented to buffer. Glows red in DATA DELETE position and data flow stops.
4	-6v, .5A	1/2 amp fuse, in series with -6 vdc secondary power from RP-32 power supply.

Table II-6. PCM Data Accumulator, Controls and Indicators (Con'td) (Figure II-8)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
5	FAN POWER indicator light	Incandescent lamp with amber jewel. Glows when power is applied to fan motors of unit.
6	TIME PRESENT indicator lights FLAG 1 FLAG 2 FLAG 3 FLAG 4	White (clear) lights, programmable through patch panel and energized by occurrence of event marker signals sent to buffer.
7	DATA PRESENT indicator light	White (clear) light energized each time data present pulse is generated.

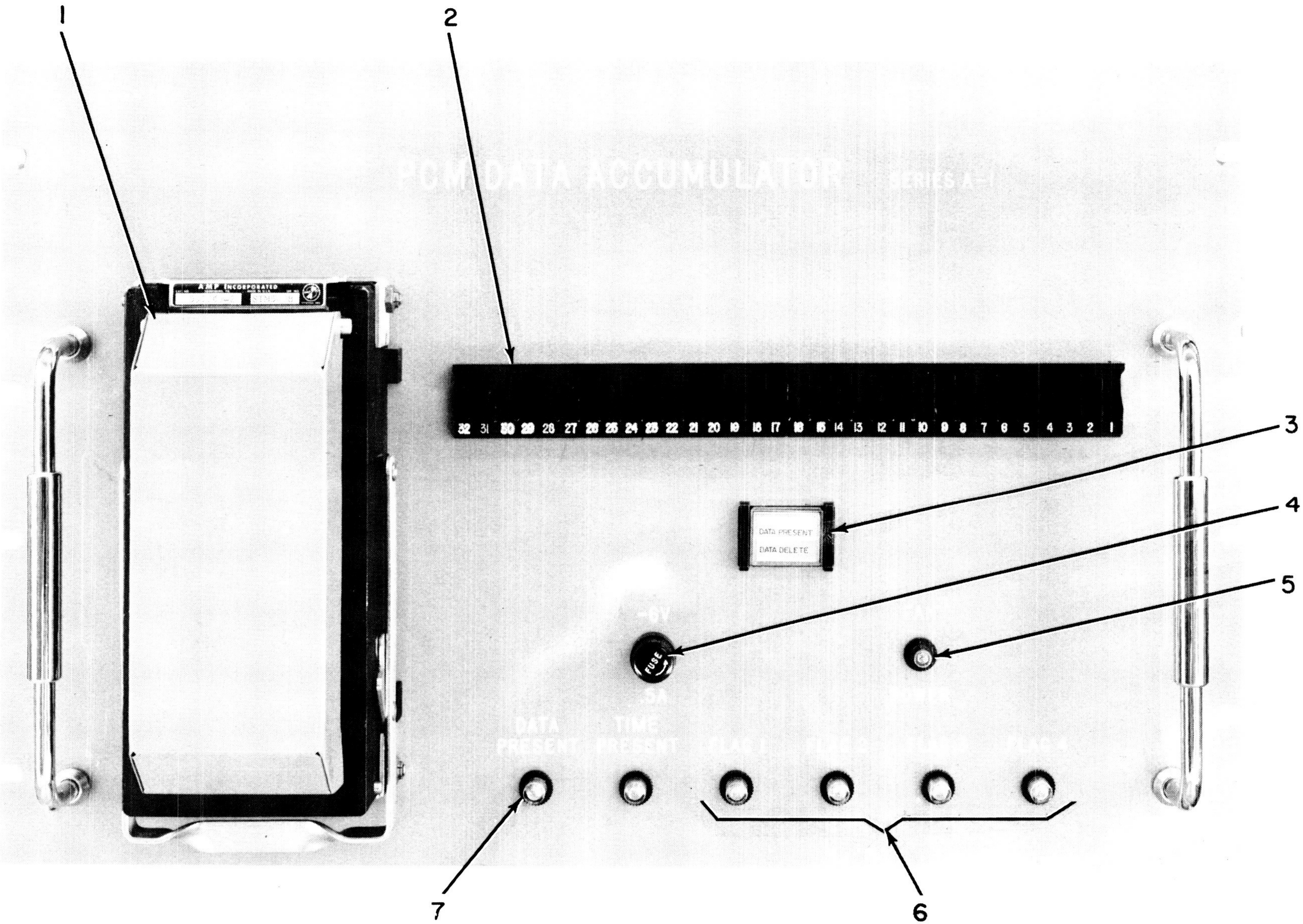


Figure II-8. PCM Data Accumulator, Controls and Indicators

Table II-7. Bits/Word/Frame Counters, Controls and Indicators (Figure II-9)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
1	Patchboard	Used to program counters according to telemetry format to be decommutated. Counter connections are made by using jumper wires between appropriate holes of patchboard.
2	BITS/WORD COUNTER WORD/FRAME COUNTER FRAMES/SUBFRAME COUNTER 1 FRAMES/SUBFRAME COUNTER 2 FRAMES/SUBFRAME COUNTER 3	Visual binary light displays, consisting of assembly of Amperex indicator triodes for each counter. Each assembly contains individual indicator for each state of counter to which it is assigned. Lighted indicator represents binary one; extinguished indicator represents binary zero. BITS/WORD COUNTER counts information bits; WORD/FRAME COUNTER counts words; each FRAMES/SUBFRAME COUNTER counts number of frames between subframes programmed.
3	FAN POWER indicator light	Incandescent lamp with amber jewel. Glows when power is applied to fan motors of unit.
4	-6v, .5A	1/2 amp fuse, in series with -6 vdc secondary power to unit from RP-32 power supply.

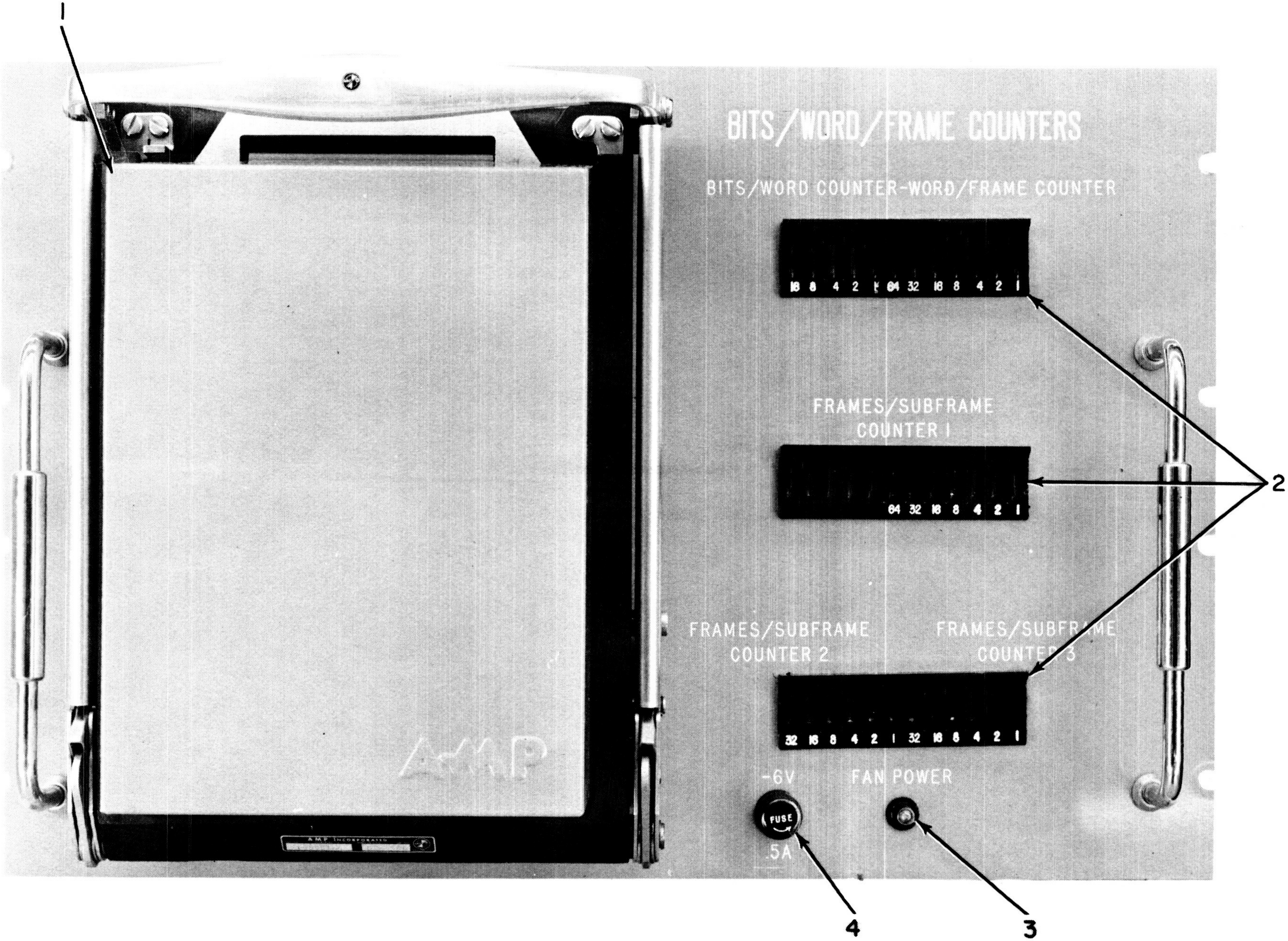


Figure II-9. Bits/Word/Frame Counter, Controls and Indicators

Table II-8. Error Monitor, Controls and Indicators (Figure II-10)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
1	Patchboard	Used to program counters of frame sync and parity error monitors, according to telemetry sync word code prescribed by format in use.
2	Indicator Light Assembly 1, 2, 4, 8, 16, 32	Group of Amperex indicator triodes, each of which is identified by binary weight of counter stage to which it is coupled, displays binary error count. Lighted indicator signifies presence of a binary one, extinguished indicator signifies presence of binary zero.
3	EXCESSIVE BIT ERROR indicator light	White (clear) light is energized when frame sync counter accumulates number of errors per frame for which ERROR SELECTOR switch is set.
4	ERROR SELECTOR switch	Rotary selector switch-off, plus six functional positions. Used to program parity, and frame sync, decision circuits. Setting of each switch determines number of errors that must be detected to generate frame sync and/or parity error alarm pulse. In OFF position, associated decision circuit is inoperative.

Table II-8. Error Monitor, Controls and Indicators (Cont'd) (Figure II-10)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
5	RESET SELECTOR AUTO/MANUAL switch	Toggle switch with two functional positions used to select operating mode of counter and decision circuit. In AUTO position counter is reset when error alarm pulse is generated. In MANUAL position error counter locks and must be manually reset when count equals or exceeds count programmed by ERROR SELECTOR switch for any frame of data.
6	PUSH TO RESET pushbutton	Used to manually reset error counter when RESET SELECTOR switch is in MANUAL position.
7	FAN POWER indicator light	Incandescent lamp with amber jewel. Glows when power is applied to fan motors of unit.
8	PARITY EXCESSIVE ERROR indicator light	White (clear) light is energized when parity counter accumulates number of errors per frame for which ERROR SELECTOR switch is set.

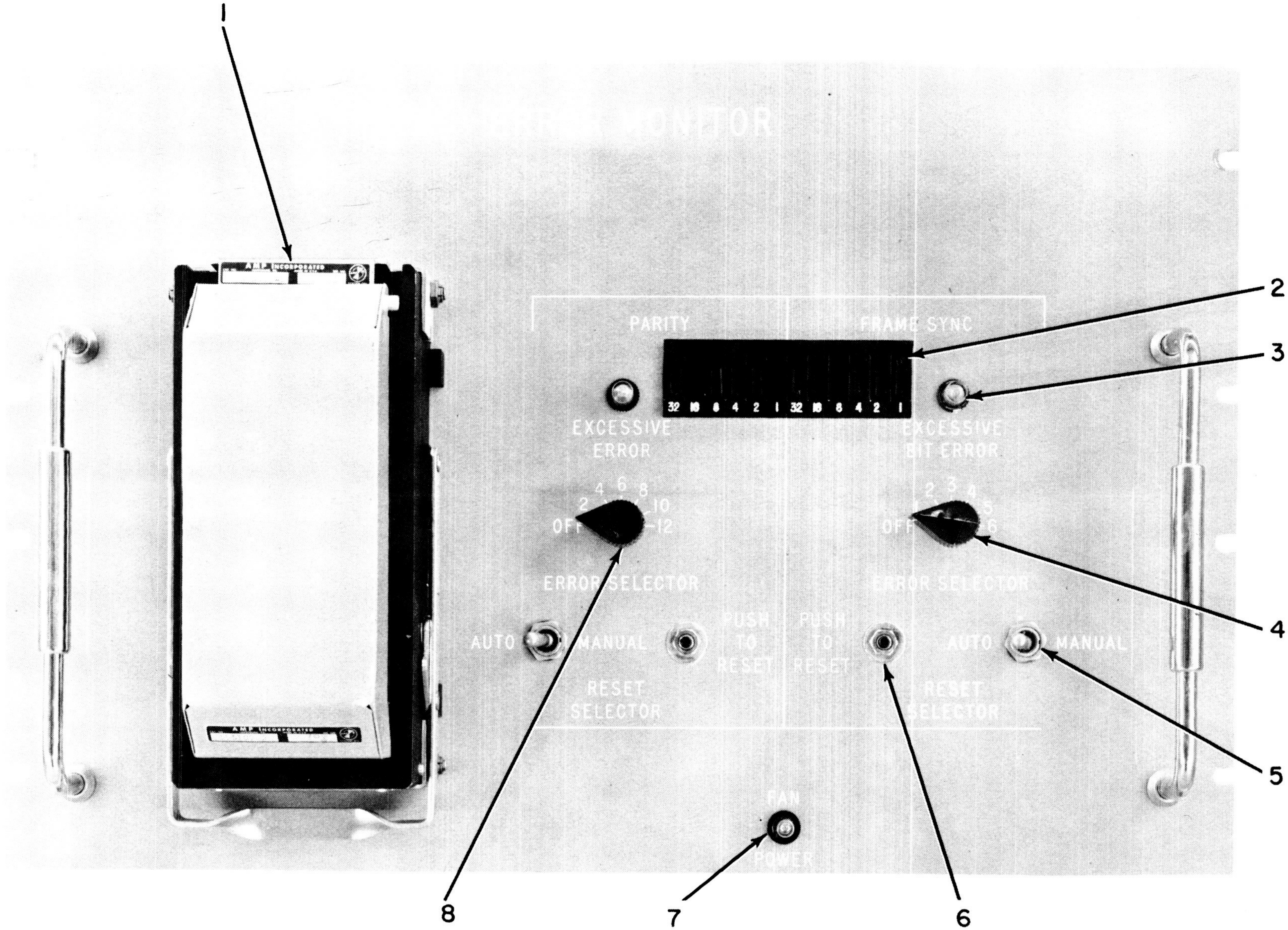


Figure II-10. Error Monitor Unit, Controls and Indicators

Table II-9. Data Quick Look Monitor, Controls and Indicators (Figure II-11)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
1	Patchboard	Used to program the binary registers, the PCM decimal display unit and the analog output jacks so that sync word errors are displayed, or so that one or more selected words per frame can be visually monitored.
2	PUSH switches	Two momentary contact push-buttons (one associated with each binary register) for manual control of each register when associated CONTINUOUS/SINGLE switch is in SINGLE position. When PUSH switch is pressed and released, count is accumulated in associated register during next frame and stored until CONTINUOUS mode is initiated.
3	CONTINUOUS/SINGLE switches	Two toggle switches (one associated with each binary register) each of which has two functional positions. In CONTINUOUS position each switch enables its associated register so that count is accumulated once per frame and held until updated during subsequent frame. In SINGLE position, switch inhibits automatic function and transfers control of register to PUSH switch.

Table II-9. Data Quick Look Monitor, Controls and Indicators (cont'd) (Figure II-11)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
4	BINARY REGISTER NO. 1 indicator assembly	Independent groups of 16 each. Amperex indicator triodes individually coupled to the binary counter stages of the data quick look monitor registers. Each group consists of 16 indicators which collectively display the binary count of a register. A lighted indicator represents the presence of a binary one and an extinguished indicator signifies a binary zero is present.
5	BINARY REGISTER NO. 2 indicator assembly	
6	ANALOG OUTPUTS jacks 1 through 8	BNC connectors, each of which provides an output signal which is the analog equivalent of a digital word.
7	FAN POWER indicator light	Incandescent lamp with amber jewel. Glows when power is applied to fan motors of unit.

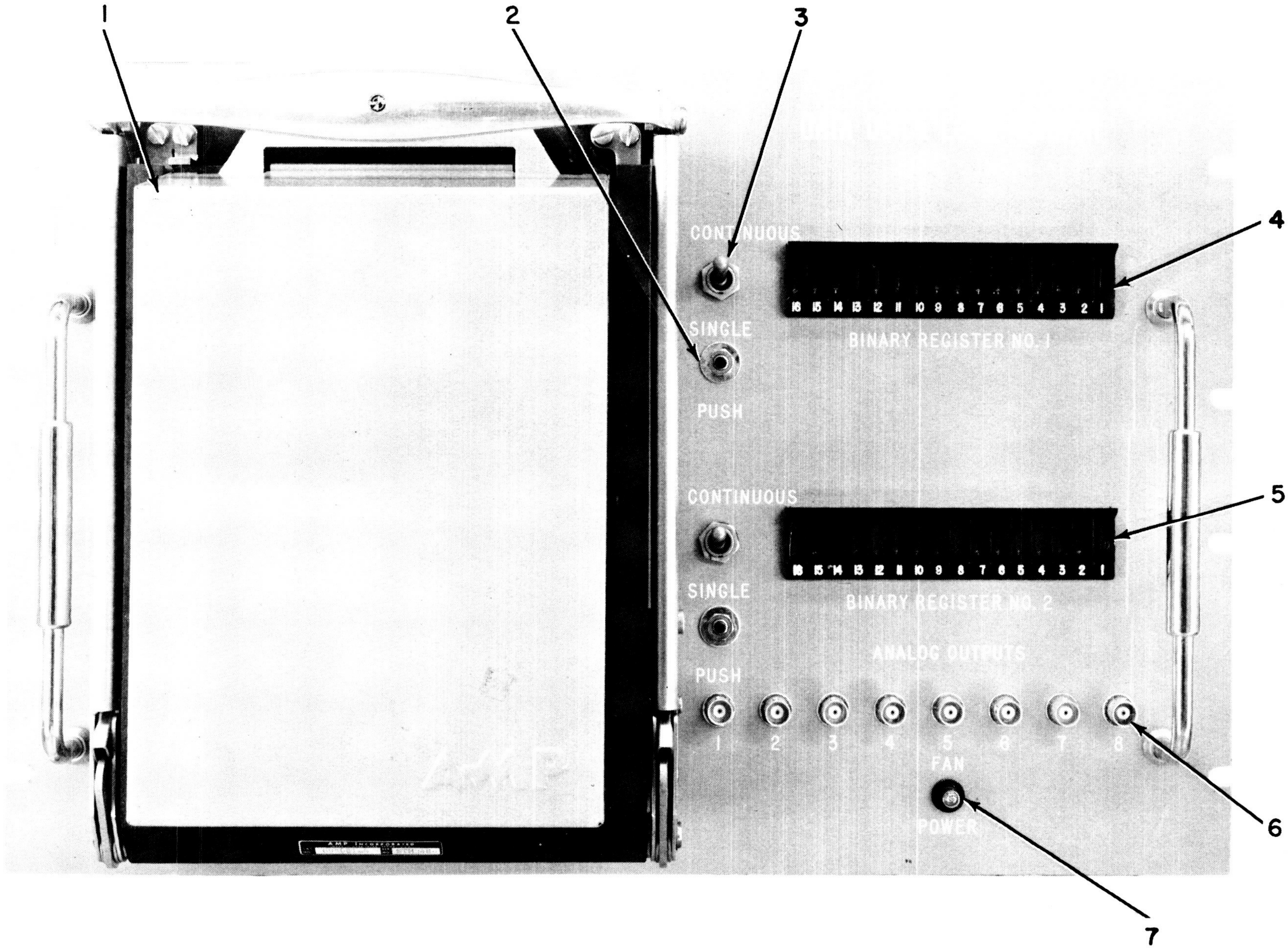


Figure II-11. Data Quick Look Monitor, Controls and Indicators

Table II-10. PCM Decimal Display Unit, Controls and Indicators (Figure II-12)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
1	WORD A WORD B	Each word display consists of 5 nixie tubes which provide optical readout for decimal equivalent of a selected digital word consisting of 16 or less information bits. Decimal equivalent of digital words consisting of more than 16 information bits can be displayed as serial value of WORD A and WORD B. Programming is accomplished by using jumper wires between the appropriate holes of the PCM Quick Look Monitor patchboard.
2	FAN POWER indicator light	Incandescent lamp with amber jewel. Glows when power is applied to fan motors of unit.

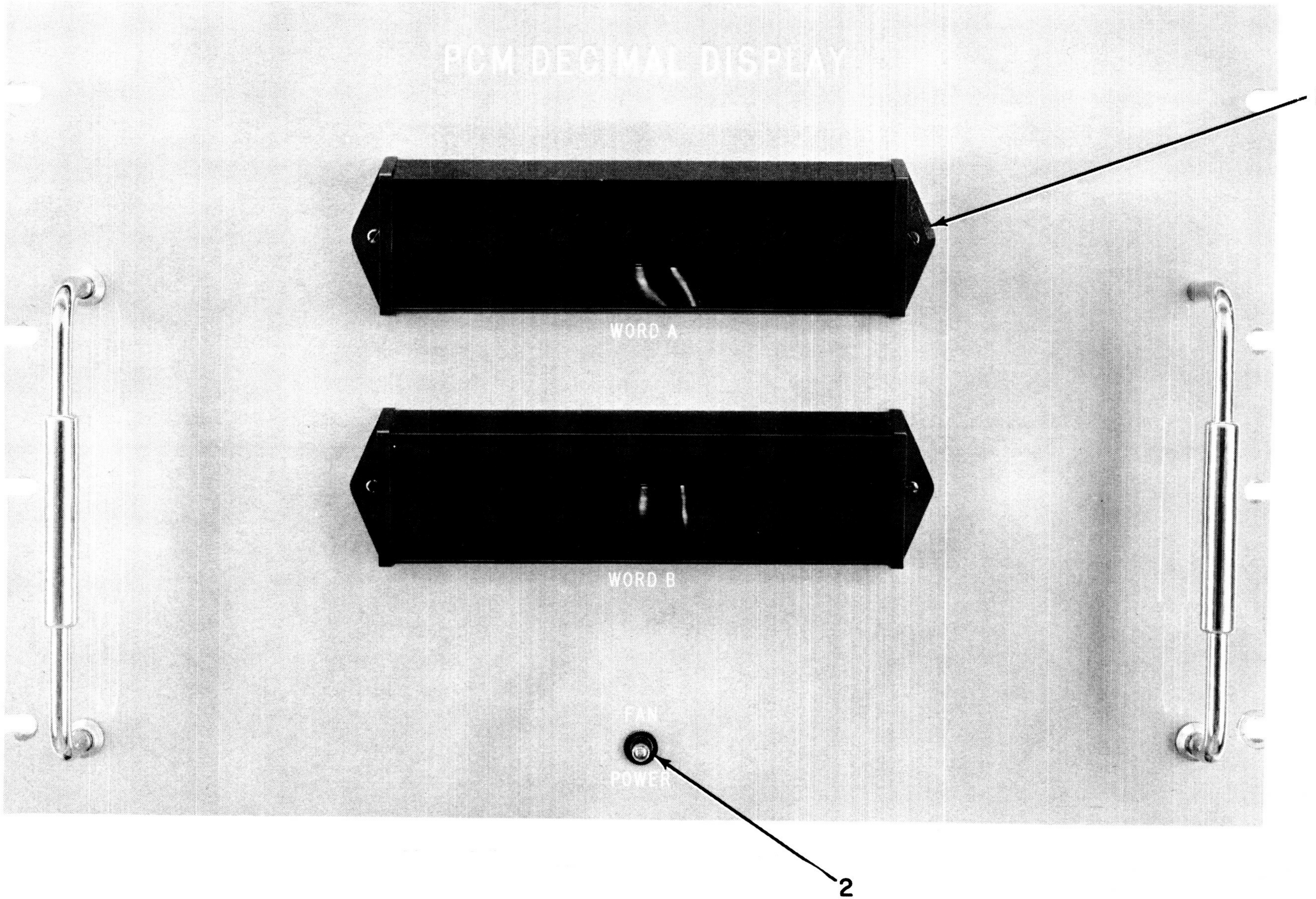


Figure II-12. PCM Decimal Display Unit, Controls and Indicators

Table II-11 Oscillograph Amplifier Unit, Controls and Indicators (Figure II-13)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
1	LEVEL 1 through 8	Individual screw driver adjustable potentiometers to regulate the gain of the individual amplifier channels.
2	INPUT 1 through 8	Individual BNC connectors which couple the input signals patched to them from the ANALOG OUTPUT jacks of the Data Quick Look Monitor, to individual amplifier channels.

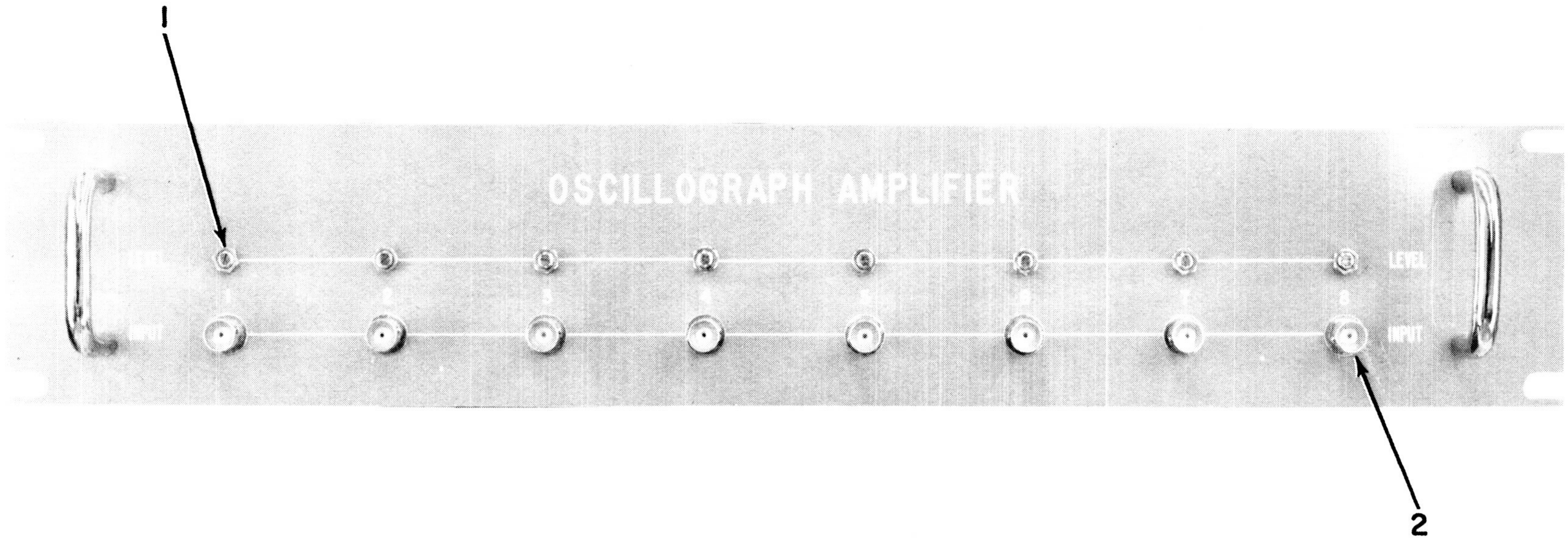


Figure II-13. Oscillograph Amplifiers Unit, Controls and Indicators

Table II-12. Recording Oscillograph, Controls and Indicators (Figure II-14)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
1	INTENSITY adjustment	Continuously variable rotary control for regulating the intensity of the light beam from the galvanometer lamp.
2	LAMP pushbutton	Momentary contact switch, used to ignite Mercury Vapor galvanometer illuminator lamp.
3	POWER ON/OFF Switch	Toggle switch, dpst, used to apply primary power to all operating circuits of unit.
4	Record speed selection switches .25, 1, 4, 16, 64	Black pushbutton switches, to regulate speed of paper transport while recording. Paper advances at .25, 1, 4, 16, or 64 inches per second when appropriate switch is pressed. Selection cannot be made unless Motor switch is in ON position.
5	Motor Switch ON/OFF	Red pushbutton press-ON, Press-OFF switch, starts and stops paper transport motor.
6	PAPER indicator	Mechanical slot-and-pointer device, indicates percent of paper supply remaining on feed roll.
7	TIMING MODE selector switch	Rotary selector switch with four functional positions. Selects locally generated timing pulses at rate of 1, 10 or 100 per second. In OFF/EXT position timing pulses can be synced to an external triggering source.

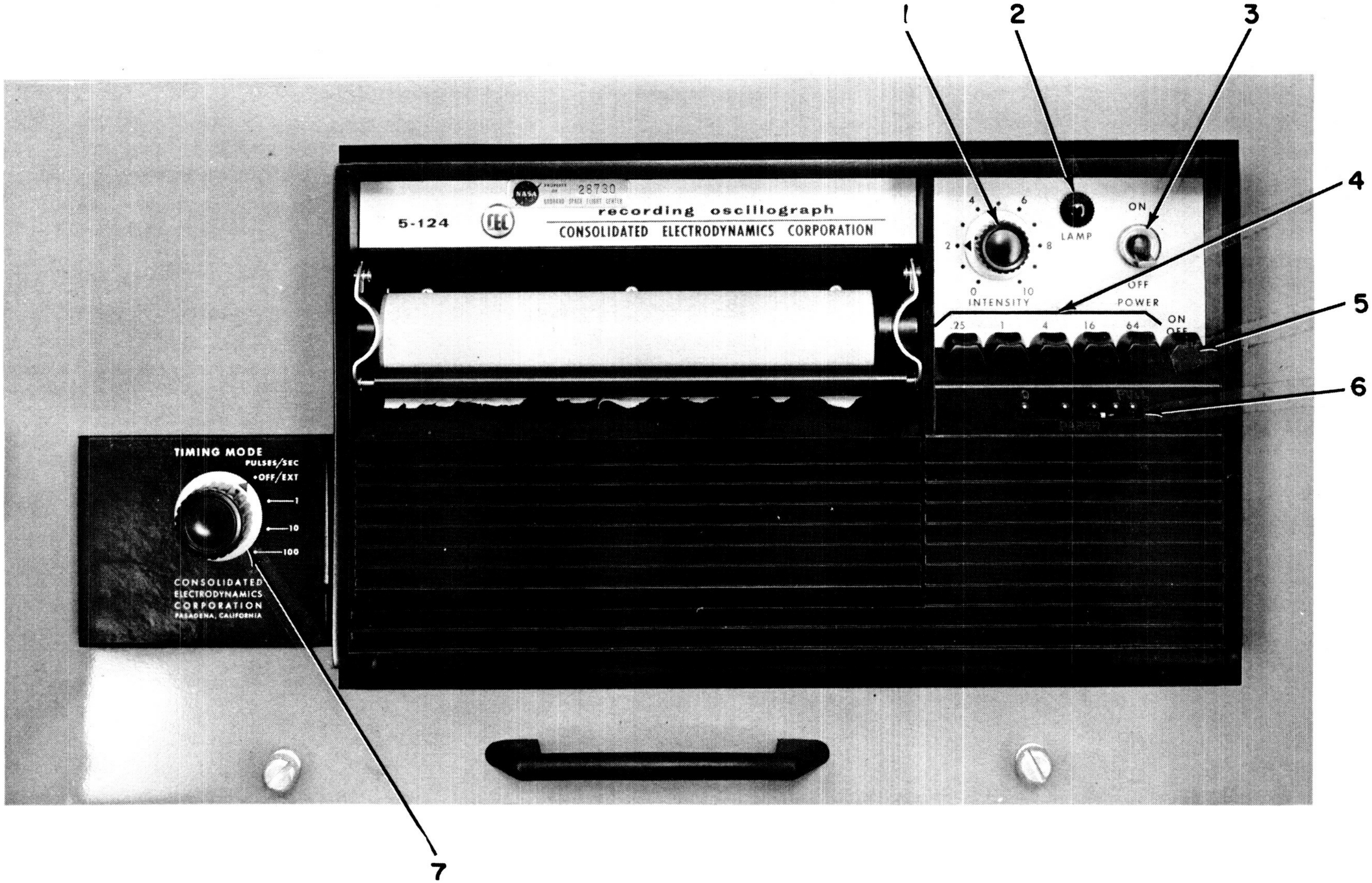


Figure II-14. Recording Oscillograph, Controls and Indicators

Table II-13. PCM Signal Simulator, Controls and Indicators (Figure II-15)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
	COMMUTATION RATE	
1	RANGE selector switch	Permits selecting commutation rate ranges from 10 to 800,000 bits/second.
2	DUTY CYCLE switch	Permits adjusting duty cycle of output pulse train from 40 to 60%.
3	FINE CONTROL	Permits adjusting internal commutation rate to desired frequency within selected range.
	RATE JITTER	
4	INT CONT (PERCENT)	Selects from 5 to 20% of internal rate jitter injected into output signal.
5	INT (60CPS) EXT	Selects internal or external jitter signal to be injected into output wavetrain.
6	COMMON WORD switches (33)	Select coding for up to 33 bits which comprise the common word in a frame. When a switch is up a "1" bit is generated. When a switch is down a "0" bit is generated.
7	POWER pushbutton	Turns on unit power. Switch glows when power is turned on.
	MISSING PULSES	
8	START WORD selector	Selects one of eight words in a frame with which to start "missing pulses."

Table II-13. PCM Signal Simulator, Controls and Indicators (Cont'd) (Figure II-15)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
9	STOP WORD selector	Selects one of eight words in a frame with which to stop "missing pulses."
10	ON/OFF/BLANKING toggle switch	Selects status of "missing pulses." In ON position, desired number of missing pulses selected at START WORD and STOP WORD switches is provided in the output pulse train. In BLANKING position, output signal will be at d-c level (baseline) when INT CONTROL pushbutton is pressed.
11	INT CONTROL pushbutton	Blanks output signal when pressed, provided ON-OFF-BLANKING switch is in the BLANKING position.
12	BLANKING (SEC) switch	Selects length of time output pulse train is blanked after INT CONTROL pushbutton is pressed or when an external signal is applied to EXT IN jack.
	NOISE	
13	LEVEL ADJUST control	Adjusts noise level superimposed on output pulse train.
14	IN/OUT toggle switch	Injects noise in-or removes noise from output pulse train.
	OUTPUT CONTROL	
15	SERIAL AMPL control	Adjusts amplitude of output serial pulse train from 0 to 10 V.

Table II-13. PCM Signal Simulator, Controls and Indicators (Cont'd) (Figure II-15)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
16	SERIAL OUT SEL switch	Selects RZ, NRZ mark "1's" or "0's", NRZ space, bi-phase or bi-polar.
17	RISE TIME control	Adjusts rise time of positive output pulses from 1 usec to 10 usec.
18	PARALLEL OUT switch	Selects type of signal (RZ or NRZ) for parallel word output.
19	SUB COMMUTATOR FRAME LENGTH switches (7)	Combinations of these seven switches select from 2 to 128 words to be contained within a subcommutated frame.
20	SPECIAL WORD LOCATION switches (7)	Determines position of special word within subcommutated frame.
21	SYNC WORD LOCATION switches (9)	Determines location of sync word for subcommutated frame.
22	SUB COM SYNC WORD switches (33)	Determines coding of subcommutated sync word.
23	SPECIAL WORD switches (33)	Determines coding of subcommutated special word.
24	WORD LENGTH switches	Consists of two selectors which select a word length of up to 33 bits per word.
25	ON/OFF toggle switch	Turns on the parity generating circuits.
26	ODD/EVEN toggle switch	Selects type of parity to be inserted at end of word; either odd or even may be selected.

Table II-13. PCM Signal Simulator, Controls and Indicators (Cont'd) (Figure II-15)

FIGURE REF. NO.	CONTROL OR INDICATOR	DESCRIPTION
27	SPECIAL WORD switches (33)	Consists of 33 switches which select coding of main commutator special word. When a switch is up, a "1" bit will be generated; when a switch is down, a "0" bit will be generated.
28	MAIN COM SYNC WORD switches (33)	Consists of 33 switches which permit selecting coding of main commutator sync word. When a switch is up, a "1" bit will be generated; when a switch is down, a "0" bit will be generated.
29	SPECIAL WORD LOCATION switches (inboard nine)	Selects position in main commutator frame for insertion of special word. Any word position in a frame may be selected for special word.
30	MAIN COMMUTATOR	
	FRAME LENGTH switches (outboard nine)	Selects number of words to be contained within a main commutator frame. Switches are labeled 1, 2, 4, 8, 32, 64, 128, and 256.

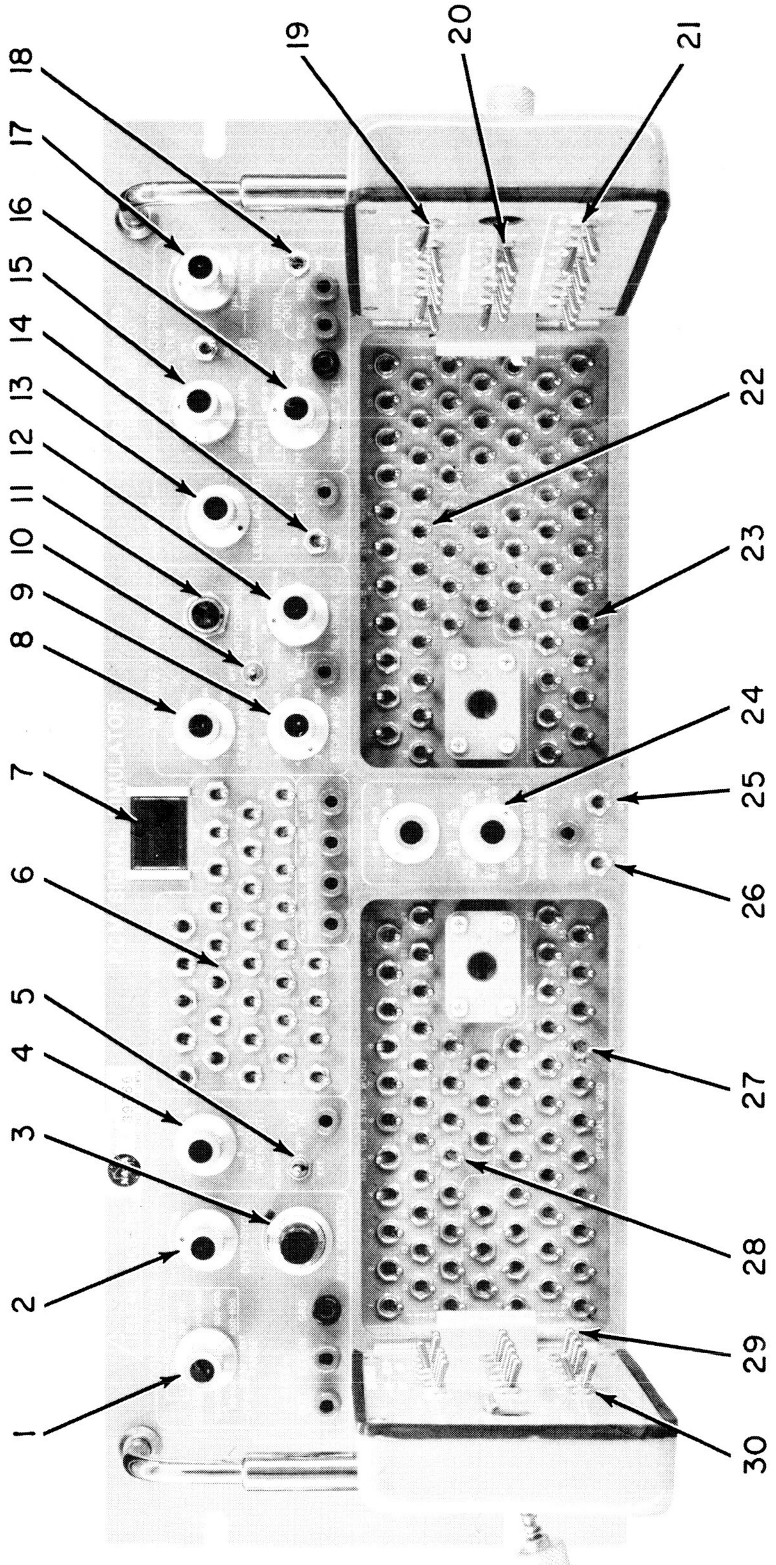


Figure II-15. PCM Signal Simulator, Controls and Indicators

C. SETUP AND OPERATING PROCEDURES

The setup and operating procedures to be performed in preparation for each operational run of the Stars PCM Data Processor system are described in the following paragraphs. When a change in the format of the telemetry signal to be processed is indicated, the programming must be revised accordingly by changing the patchboards, which comprise the processor instruction center. The procedural steps given here are based on the assumption that spare patchboards have been prepared in anticipation of the signal to be processed.

CAUTION

> Patchboards should not be inserted in their holders, or removed therefrom, when power is applied, since the making and breaking of the circuits they control can generate transients capable of damaging the associated transistors and diodes.

Once the patchboards have been installed and power has been applied, a fifteen minute warm up period should be observed to allow operating parameters to stabilize before the additional setup procedures are performed.

GENERAL INSTRUCTIONS

a. With system power switch in OFF position, select pre-programmed patchboards for signal to be processed and insert them in their proper places on racks B and C.

b. Press and release PCM POWER switch on Control and Indicator Panel, rack B. POWER switch plate glows green when primary power is applied.

c. Make sure that all other power switches are on. The meter on each panel should indicate 110-125 volts ac, and all three meters should indicate the same rms value, ±5%.

d. Check to be sure FAN POWER indicator lights on the panels of the appropriate units are energized. A FAN POWER indicator light is located on the front panel of the PCM Decimal Display, the Data Quick Look Monitor, the Error Monitor, the PCM Search and Lock, the PCM Data Accumulator, and the Bits/Word/Frame Counters.

e. Observe READY light on front panel of the Digital Signal Synchronizer (rack C). This light glows green when synchronizer circuits are energized.

f. Allow a 15-minute warm up period to elapse for stabilization of operating parameters. During the warm-up period, make the following adjustments and observations:

1. Select the desired operating mode for the Data Quick Look Monitor with the CONTINUOUS/ SINGLE switches on the front panel of the unit.

2. Select the desired operating mode for the Error Monitor with the RESET SELECTOR AUTO/ MANUAL switches for PARITY and FRAME SYNC on the front panel of that unit.

3. Rotate the PARITY and FRAME SYNC ERROR SELECTOR switches on the front panel of the Error Monitor unit to program the error counters as desired.

4. Observe the TEMPERATURE LIMITS indicators on the Control and Indicator Panel of rack B at frequent intervals for indications of overheating. If an overtemperature indication is observed, immediately remove secondary power from the rack affected by reversing the procedure of step e. 1.

SECTION III

THEORY OF OPERATION

A. INTRODUCTION

This section describes the function and theory of operation of the GSFC-designed units comprising the STARS PCM Data Processor. The Bit Synchronizer and Simulator Units are described in their respective manuals provided by the vendor.

In the following discussion reference is made to functional drawings included at the end of every unit section. Figure III-1 explains the circuit symbols and signal designations used in all drawings*(figures). It should be noted that the input-output line relationship in FA's and DM's or DMA's is collinear, meaning that a trigger on the input line will produce a true (-6 VDC) output on the output line collinear with the input line, and a false (0 VDC) output on the other output line.

The theory of operation is presented in terms of logical functions which are performed by the circuits involved without detail explanation of the actual circuits. It is assumed that the reader is or will have acquainted himself with the basic function and operation of logic circuits such as flip-flop, one shot, gate, etc. A detail description of circuits used herein is given in the Computer Control Company's (3c) Instruction Manual For S-PAC Digital Modules, dated 8 July 1963, and Section V of this manual.

In reference to FA and BC circuits, the terms Set and Reset are used to designate the state of the output lines used. Set means "true" and Reset means "false" output. When a counter is said to be "reset" it means that all of its "true" outputs used are forced to assume 0 vdc. In some cases particular output pins are referred to as being set or reset. Also, the set or reset side of an FA is arbitrarily designated by the vendor as indicated in the S-PAC manual. This convention is not always followed herein.

Each subsection is preceded by a functional description of the unit, explaining what the particular unit does in relation to the overall system and the specific functions generated therein. The units covered in this section are: Search and Lock, B/W/F Counters, Accumulator, Decimal Display, Quick Look, and Error Monitor. The first three units function in conjunction with each other to generate the required signals. Therefore, when reading about one of them, the reader may have to refer to figures and text describing the others as well to find the source of certain signals mentioned therein. The other three units function independently.

*(NOTE: Reference should be made to Fig. III-35, Page III-66, for definition of symbols used throughout this Section.)

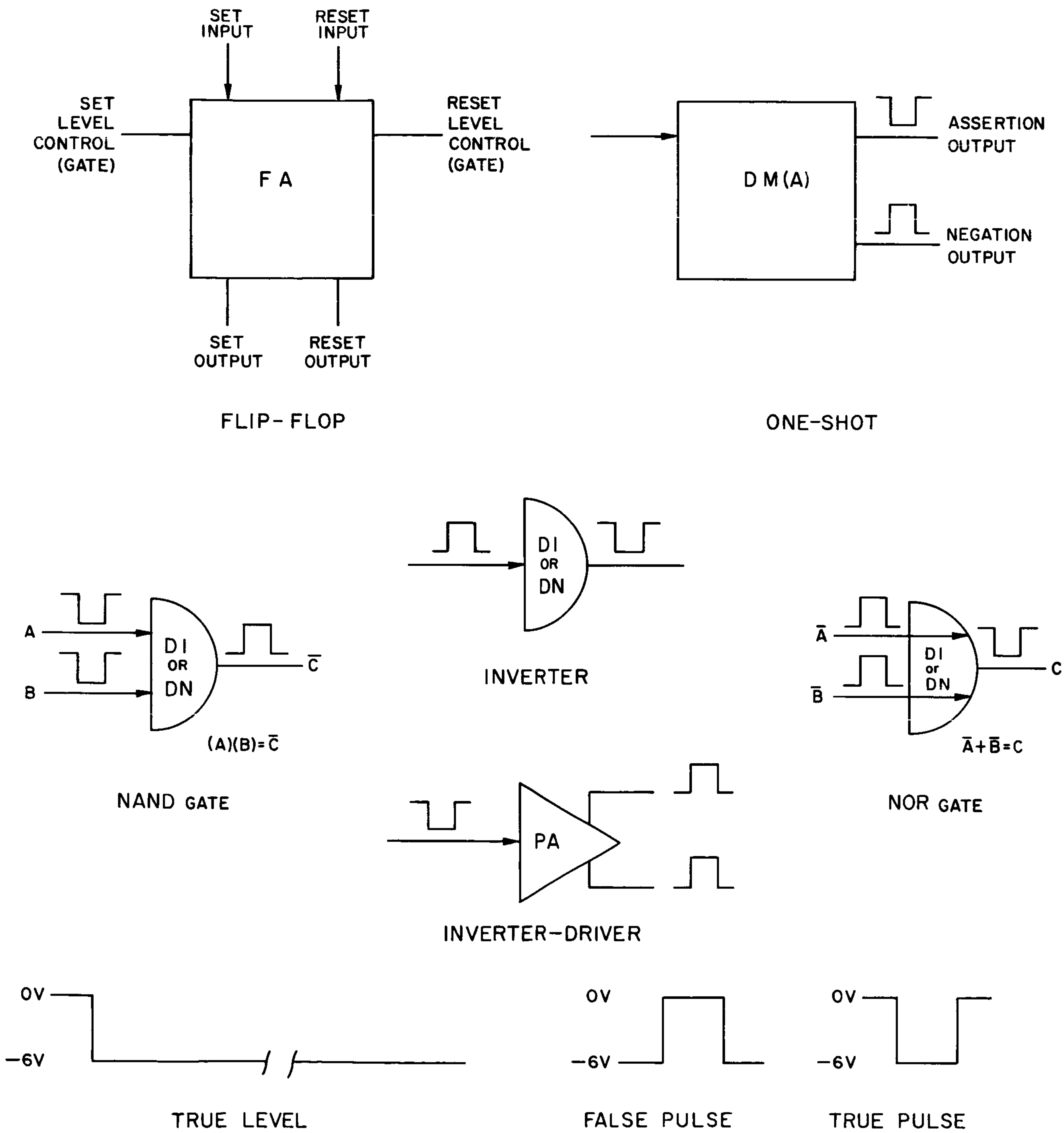


Figure III-1. Circuit Symbols and Signal Designation

B. SEARCH AND LOCK UNIT

FUNCTIONAL DESCRIPTION

The primary function of the search and lock unit is to lock the system in synchronization with the input PCM data train. Until frame (or word) sync is acquired the unit holds the system in a search condition. As long as the system is in this condition data cannot be passed to the STARS buffer. To acquire frame sync the search and lock unit operates in conjunction with the bits/word/frame counters unit which sends pulses indicating the occurrence of frame sync words. When a programmed number of frame sync patterns are recognized in the search and lock unit in coincidence with the frame sync words, the system is locked in synchronization with the input data.

If, after frame sync has been acquired, frame sync pulses are missed, the search and lock unit will flywheel through a programmed number of missed or invalid frame sync pulses before reverting to the search condition. Reacquisition of frame sync once the system is in the search condition is done automatically.

Although seldom used, the search and lock unit has circuits for the acquisition of word sync. When word sync is used, it is first necessary to acquire word sync and then frame sync before the lock level is generated. The system remains in the search condition until this occurs. The word sync pattern is recognized in the search and lock unit. It must occur in coincidence with a programmed number of end of word pulses from the bits/word/frame counters unit for the acquisition of word sync. The flywheel function also operates for word sync.

In addition to the search and lock operation the search and lock unit also performs several other functions. It converts the serial input data train into parallel form for use by the word sync, frame sync, and subcom sync recognizers, and for distribution through the remainder of the system and to the buffer; it generates 2-usec pulses from the input clock signal which are counted in the bits/word/frame counters unit to determine end of word and the occurrence of frame sync and subcom words, and which are used as strobe pulses throughout the system; it automatically reverses the polarity of the input data when it is determined to be out of phase with the clock signal; and it generates a reset pulse for the entire system.

THEORY OF OPERATION

Strobe and Clock Pulse Generation

Strobe and clock pulses are derived from the input clock signal by the strobe generator circuit shown in figure III-2. The clock signal is derived from the input data supplied by the bit synchronizer, and occurs at the data bit rate. The input clock signal is inverted at DI3-27 and then applied to DM5-9 and DM6-22. Due to a second inversion at DI3-16, the DM's will be alternately triggered by the leading and trailing edge of every clock pulse. The assertion output of DM5 (pin 17) is designated C', and the negation output (pin 28) is designated $\overline{C'}$ (both of which are strobe pulses); the assertion output of DM6 (pin 10) is designated CD, and the negation output is designated $\overline{CD}$. The CD pulses trail the C' pulses by 180°. The phase and polarity relationship between the various pulses derived from the clock signal is also shown in figure III-2.

Search and Lock Function

The acquisition of frame sync requires the coincident occurrence of a programmed number of frame sync recognition pulses with the proper frame sync word (or words). When this occurs the system is then locked in sync with the input data train. Until this time the system is searching for frame sync. If the satellite whose data is being processed uses word sync, then this must be acquired before frame sync. The system does not go to the lock condition until both have been acquired. In the discussion of the search and lock unit which follows the more usual case in which the satellite uses frame sync only will be considered first, followed by the sequence of operations when word sync is also used. It will be assumed initially that the input data is in phase with the clock signal, and then the case of out-of-phase data will be discussed.

The frame sync pattern is detected by the in-phase frame sync recognizer (fig. III-3) which puts out a frame sync pulse (FS) each time the pattern is recognized. The inputs to the in-phase recognizer are obtained from the main shift register (serial-to-parallel converter, fig. III-4) by patching them to the proper shift register stages (complements of the frame sync pattern) so that all inputs will be "zeros" when the frame sync pattern appears without errors. As an example, assume that a satellite uses the eight-bit frame sync pattern shown in figure III-1. The recognizer would then be patched into the stages of the shift register specified in the figure. (For definition of true-false outputs of shift register stages see paragraph on Serial to Parallel Data Conversion.) Patching into the shift register must be done so that the least significant bit of the frame sync pattern is patched into the least significant bit stage of the shift register, and succeeding bits into corresponding shift register stages. The order of patching into the recognizer is not important, however, recognizer inputs which are in excess of a particular satellite's frame sync pattern must be patched to ground. A frame sync recognition pattern of up to 32 bits can be accommodated.

The recognizer may be programmed to tolerate from zero to five bit errors in the frame sync pattern and still provide FS pulses. This is done by patching -6 volts to the appropriate patch point on the error detector cards. These cards are designed by GSFC and are discussed in Section V, Special Circuits.

The DI's in series with each input to the error detectors invert the signals so that errors in the frame sync pattern will appear as "ones" at the error detectors. If the number of "ones" does not exceed the allowable number of errors for which the recognizer is programmed, the output from the error detector will be an analog signal more negative than -1.5 volts, the threshold voltage of the ST. This triggers the ST and a FS pulse is generated. When there are more errors than the error detector is programmed to accommodate, the output from the detector varies between zero and -1.5 volts, and no FS pulses are produced.

FS pulses are checked in the in-phase frame sync circuit (fig. III-5) for coincidence with frame sync word (FSW) pulses supplied by the words/frame counter of the bits/word/frame counters unit. When the programmed number of FS and FSW pulses appear in coincidence, the frame sync circuit generates a word and frame lock level (WFL) which locks the data processor in sync with the input data. While searching for frame sync three discrete combinations of signals can occur: (1) (FS)(FSW'); (2) $(\overline{FS})$(FSW); and (3) (FS)(FSW). The first two comprise the search pulses, and the third is the lock pulse, the only valid combination of two signals occurring in coincidence.

The in-phase frame sync circuit contains a search counter which speeds up the acquisition of frame sync by continuously presetting the words/frame counter until the frame sync pulse appears in the proper word, and a lock counter which gives confidence that frame sync pulses which do appear in the proper word are valid by counting a selected number before generating WFL. The search counter also acts as a flywheel once the system is in sync.

The output of the search counter is patched to the search gate for the initial search function, and to the flywheel gate for the flywheel function. For the search function, the search counter is set for a smaller number of counts than the lock counter. Before frame sync is acquired FS and FSW' pulses (invalid frame sync words) are gated together as the input to the counter. When the selected number of these pulses occur (usually a very small number) DN7-21 goes positive. This results in a $\overline{FR}$ pulse which presets the words/frame counter to the correct count, and resets both the search and lock counters. The process is repeated until FS and FSW appear in coincidence.

Note that the first FS pulse is gated through DI9-25 and passes out DI10-23 as a $\overline{FR}$ pulse which presets the words/frame counter. This is done on the assumption that the initial FS pulse is a "good" pulse. Consequently, the Data Processor will, in most cases, go into sync faster with a minimum loss of data. If the assumption proves to be incorrect the search counter will preset the words/frame counter in the usual manner until the FS and FSW pulses occur simultaneously. The positive-going trailing edge of the first FS pulse at FA6-22 resets the flip-flop. This puts DI9-18 at the "zero" level which prevents following FS pulses from being gated through. This condition prevails until the flip-flop is returned to the set condition by an external reset $(\overline{ER})$ pulse or by the loss of frame sync.

The output of the lock counter is patched to NAND gate inputs U-18, -20, -22, or -24 so that the gate is enabled after a selected number of gated FS and FSW pulses have been counted. These gated pulses indicate that the frame sync pulses are appearing in coincidence with the proper frame sync word. When DN8-9 goes positive FA6-27 goes to the "one" level. The system is now in sync with the input data and WFL is sent to the accumulator unit and the bits/ word/ frame counters unit so that processing of data can now begin. If word sync is used, word lock level is patched to C-23 where it is gated with frame lock level to produce WFL.

When the lock counter reaches the selected count, it and the search counter are reset. Also note that the gated FS and FSW pulses from DI10-34 result in $\overline{\text{FR}}$ pulses which preset the words/frame counter each time they occur.

If frame sync pulses are missed after the system is in sync, the search counter performs the flywheel function until a selected number of missed pulses occurs. At this time frame lock is lost and the search counter resumes the search function.

When the frame lock level is obtained DN7-34 and DN7-19 go to the "zero" level. This inhibits both gates so that the input to the search counter is the gate with $\overline{\text{FS}}$, FSW and frame lock level as inputs, and the output from the counter is through the flywheel gate. Each time a FSW pulse occurs without a coincident FS pulse, the counter advances by a count of one. The system will then flywheel until the programmed number of missed FS pulses occur. If this happens DN7-17 goes positive. This causes a positive transition at FA6-29 which returns the flip-flop to the set condition. WFL is now lost so that no additional data can be dumped into the output register in the accumulator unit, and a dump command is sent to the buffer. The search and lock counters are also reset and the words/frame counter is again preset. The normal search function now resumes to reacquire frame sync.

In case the satellite whose data is being processed uses word sync, then word sync must be acquired before frame sync. Both are required to generate WFL and place the system in the lock condition.

The acquisition of word sync requires that a programmed number of word sync pulses (WS) occur in coincidence with end of word pulses (EWP) from the bits/word counter of the bits/word/frame counters unit. While searching for word sync three discrete combinations of signals can occur: (1) (WS)(EW'); (2) ($\overline{\text{WS}}$)(EW); and (3) (WS)(EW). The first two comprise search pulses, and the third is the lock pulse, the only valid combination of two signals occurring in coincidence.

Word sync pulses are detected by the recognizer circuit shown in figure III-6. Both the in-phase and out-of-phase recognizers are shown in the figure. A word sync pattern of up to three bits can be accommodated. The recognizers can be patched to tolerate one bit error and still put out a word sync pulse. The in-phase recognizer provides both the word sync pulse, WS, or its complement, $\overline{\text{WS}}$.

In-phase inputs are patched to points in the main shift register which will give all "ones" when the word sync pattern occurs. The out-of-phase inputs are patched to the complementary bit positions so that if the input data is initially out of phase with the clock the sync pattern will be recognized in this circuit. If the input data is initially in phase DN19-31 goes positive when the word sync pattern occurs without errors, and DN21-21 goes negative when the pattern occurs with one error (or no errors). If the input data is initially out of phase, DN20-21 goes positive when the sync pattern occurs without errors, and DN21-7 goes negative when the pattern occurs with one error (or no errors). Note that the outputs which allow one bit error also provide a word sync pulse if there are no errors.

Word sync pulses and end of word pulses are compared for coincidence in the in-phase word sync circuit (fig. III-8). It is identical in construction and function to the in-phase frame sync circuit.

Inputs to the search counter for the initial search function are gated WS and EW' pulses. For the flywheel function the inputs to the counter are gated $\overline{WS}$ and EW pulses and word lock level. The lock counter receives gated WS and EW pulses for its input. The first WS pulse received results in a $\overline{WR}$ pulse which resets the bits/word counter. Word lock is obtained when a positive transition occurs at FA6-26.

WL is gated with frame lock to produce WFL, thus both word and frame sync must be acquired before the Data Processor can be locked in sync with the input data.

When the input data train is initially out of phase with the clock signal, the frame sync (or word sync) pattern is detected in the out-of-phase recognizers and compared for coincidence with FSW (or EW) pulses in the out-of-phase frame or word sync circuit. The out-of-phase frame sync recognizer is shown in figure III-3. It is patched to the true bit positions of the frame sync pattern in the main shift register so that the inputs will be all "zeros" if the frame sync pattern appears without errors, but out of phase with the clock. Operation of the out-of-phase recognizer is identical to that of the in-phase recognizer discussed above. The out-of-phase word sync recognizer has also been discussed above in connection with the in-phase word sync recognizer.

Figure III-7 is the logic diagram for the out-of-phase frame or word sync circuit. When word sync is used it performs the search and lock function to obtain word sync only. If word sync is not used, it performs the same function to obtain frame sync. In addition, it generates a signal which reverses the phase of the input data when the search and lock function is completed.

The operation of the out-of-phase frame or word sync circuit is almost identical to that of the in-phase frame and word sync circuits except that it does not perform the flywheel function. This is not necessary as the circuit does not operate after it completes the search and lock operation and reverses the polarity of the input data. The in-phase and out-of-phase search counters and lock counters are set for the same number of counts.

If word sync is used the input to the search counter is gated WS' and EW' pulses, and to the lock counter, gated WS' and EW pulses. When only frame sync is used, the search counter receives gated FS' and FSW' pulses, and the lock counter gated FS' and FSW pulses. The $\overline{FR/WR}$ pulses are used to reset the words/frame counter when only frame sync is used, and the bits/word counter when word sync is used.

A positive transition occurs at FA16-26 when the lock counter has counted the programmed number of gated WS' and EW or FS' and FSW pulses. This causes FA16-27 to go to the "one" level. The positive transition which occurs at FA16-28 as this happens triggers DM14 which puts out a search pulse. When only frame sync is used, the search pulse is patched to point C-18 in the in-phase frame sync circuit so that WFL is generated when the search pulse is received. If word sync is used the search pulse is patched to point C-19 in the in-phase word sync circuit. When the search pulse is received WL is generated, and the search and lock function to acquire frame sync then begins. The search pulse is also fed back to FA16-29 to reset the flip-flop.

The positive transition at FA16-28 also causes a reversal of the polarity of the input data, so that search and lock operations will now be performed by the in-phase frame sync circuit only.

Serial to Parallel Data Conversion

The main shift register (fig. III-4) receives data in serial form from the output of data polarity inverter circuit (fig. III-2) and distributes it in parallel form through the system and to the buffer. Data is also required in parallel form by the frame and word sync recognizers in the search and lock unit. The shift register contains 32 stages (2^0 through 2^{31}) with the least significant bit stage connected to the output of the data polarity inverter. The set output of each stage is designated the true stage, and the reset output is designated the false output. Note that the true outputs are connected to even numbered patch points (V2 and U2 for the 2^0 stage) and that the false outputs are connected to odd numbered patch points (V1 and V2 for the 2^0 stage).

Data is strobed into the shift register at SR11-23 and -24, the level control inputs, during the latter half of each data bit by $\overline{C}'$ pulses. The level control inputs are active when at the "zero" level. To set a "one", for example, into this stage, the set level control must be at the "zero" level when the strobe pulse arrives. Once a bit has been set in the first stage it is shifted through the register by succeeding $\overline{C}'$ pulses.

The set output of each stage is fed to the shift register output power amplifiers located in the error monitor unit. Amperex indicator triodes connected to the reset output of each stage monitor the contents of the register.

Data Polarity Inversion

When the input data is not in phase with the input clock signal the polarity of the data must be reversed. The in-phase condition of the input data is defined with respect to the clock signal, and is illustrated in figure III-2. This figure also shows the polarity inverter circuit.

When the input signal is any type other than modified biphase, patch points A1 and C15 are connected, as are points D16 and C17. Assuming that initially FA7-28 is at the "one" level, the input data will be gated through DI2-19 and then through DI2-11. As a result of the additional inversion of the signal through the latter gate, the output signal at DI3-33 is reversed in polarity with respect to the signal at DI2-33. With the signal polarities shown at this point in figure III-2, a "one" will be strobed into the first stage of the shift register.

If it is determined that the input data is out of phase with the clock signal, a positive-going signal will be received from the out-of-phase frame or word sync circuit which is applied to FA7-24 and -26. This triggers the flip-flop and FA7-27 goes to the "one" level. Outputs from DI2-6 and DI2-16 are now inhibited, and the input data is gated through DI3-20 and DI2-9. As a result, the polarities of the signals at DI2-23 and DI3-33 are reversed.

If the input data is modified biphase-coded, patch point A2 is connected to C15, and D17 is connected to C17. To accommodate it the synchronizer is set for a NRZ-C signal at twice the bit rate of the incoming data. This results in a clock signal at twice the bit rate which must be divided by two in the search and lock unit. To accomplish this the input clock signal is fed through a flip-flop before being applied to DM5-9 and DM6-22. The modified biphase data is passed through a conversion circuit so that the output at FA7-7 is a standard biphase signal.

System Reset

The system reset circuit is shown in figure III-6. It consists of a voltage divider network, a ST, and a PA. Depressing the reset push button switch causes a positive transition to occur at ST22-17. This results in a negative pulse from the ST. The pulse is inverted by the PA, which drives the external reset lines in this and other units.

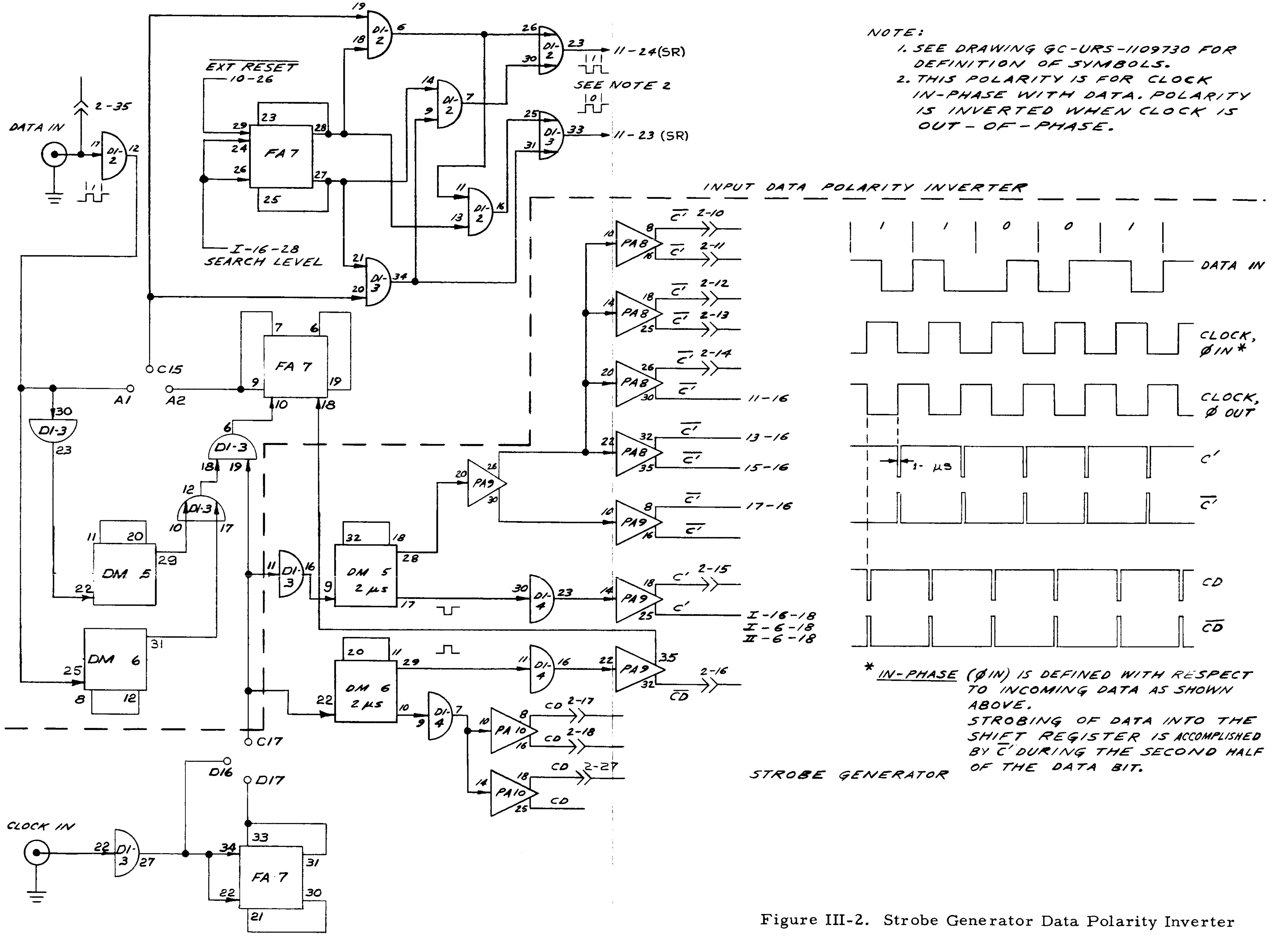


Figure III-2. Strobe Generator Data Polarity Inverter

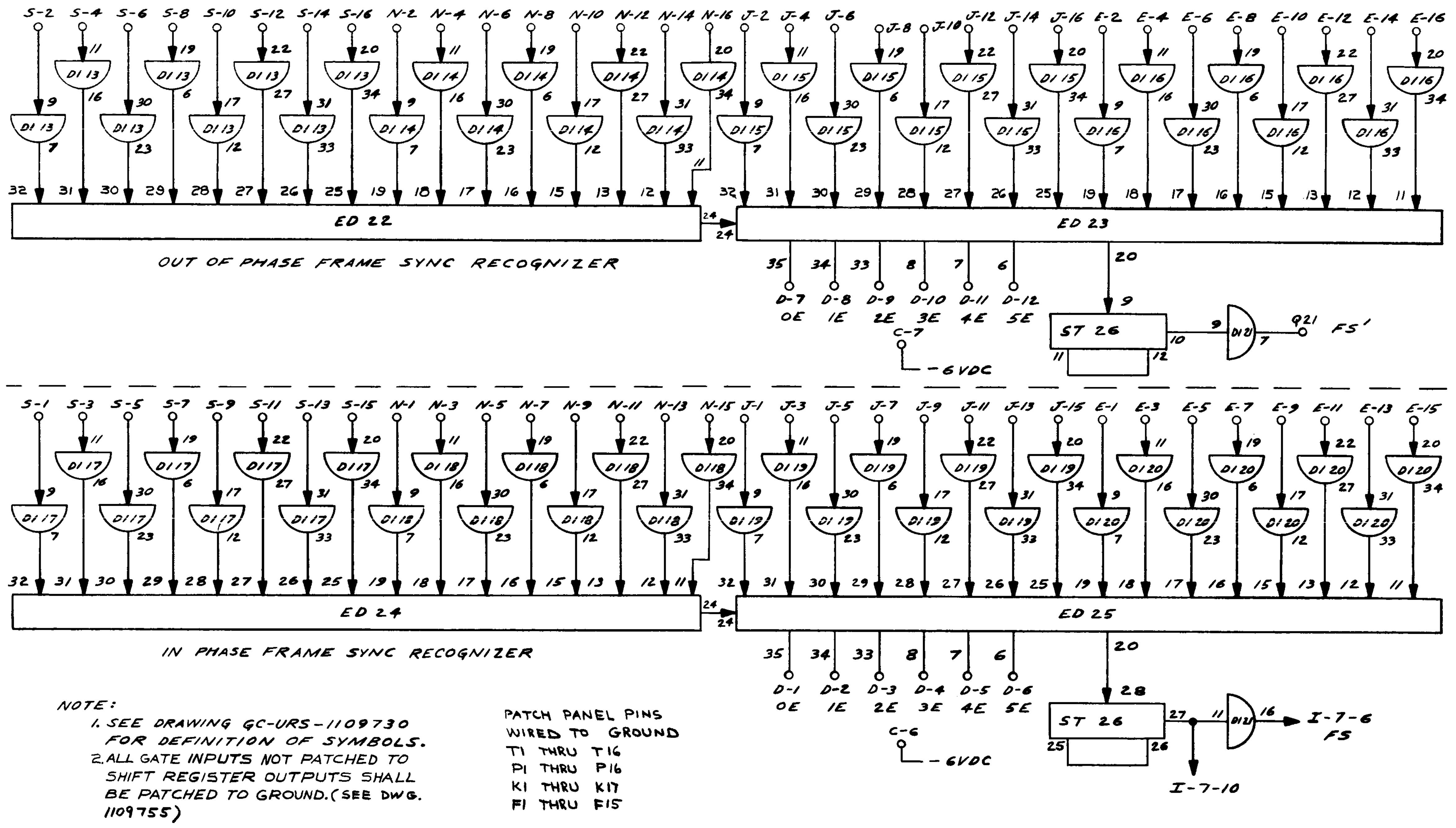
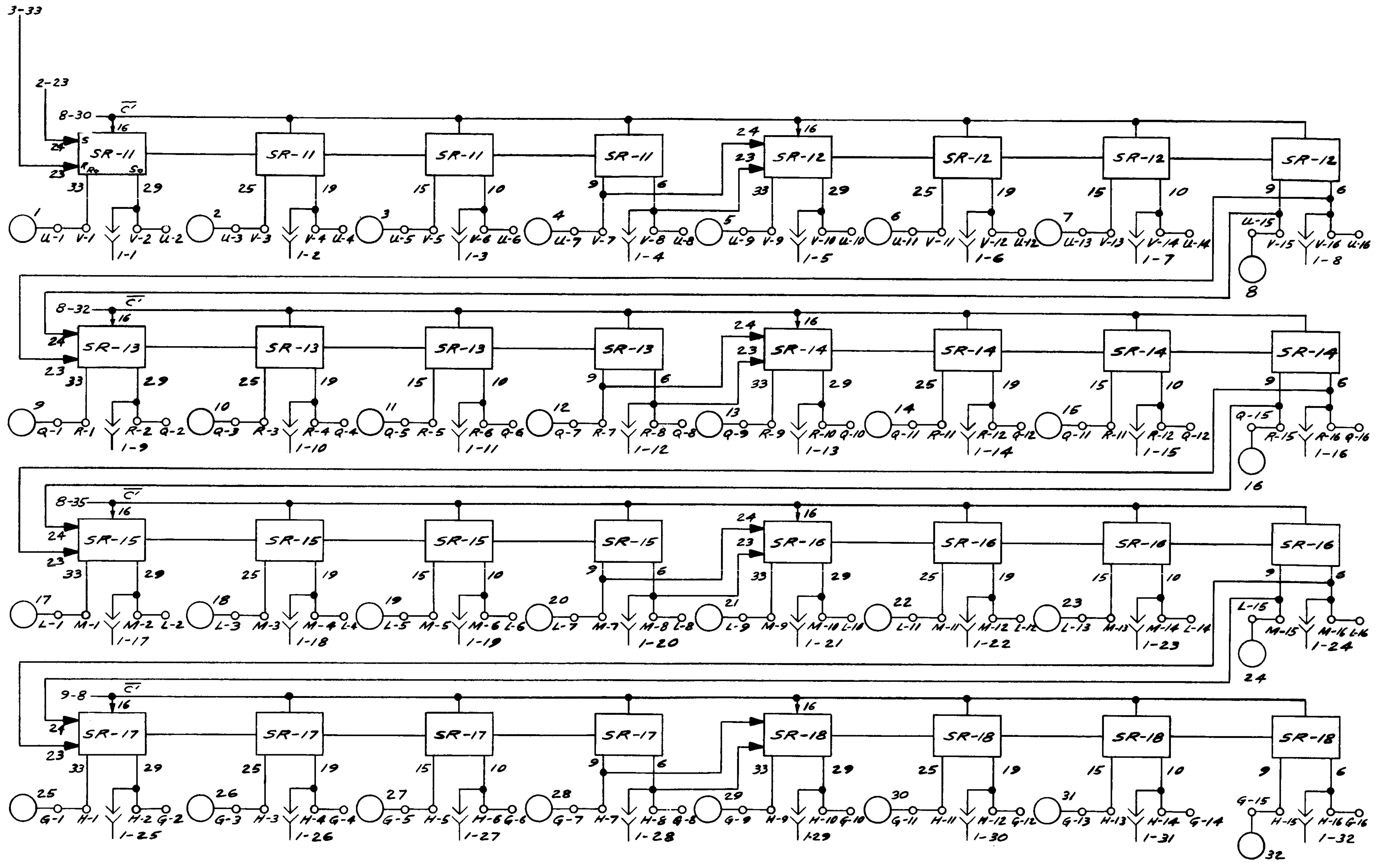


Figure III-3. Frame Sync Recognizers



NOTE:
1. SEE DRAWING GC-URS-1109730
FOR DEFINITION OF SYMBOLS.

Figure III-4. Serial-to-Parallel Converter

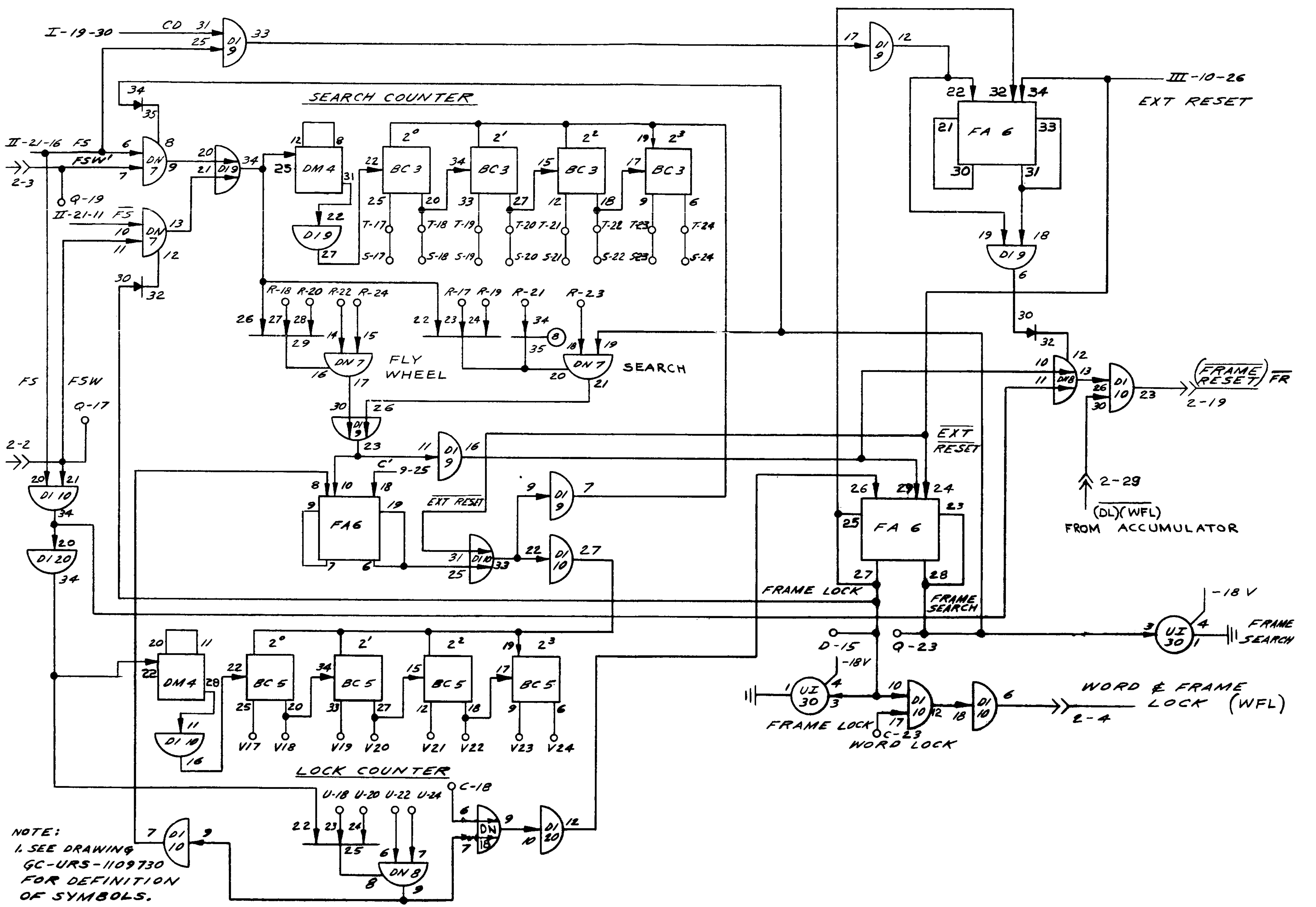
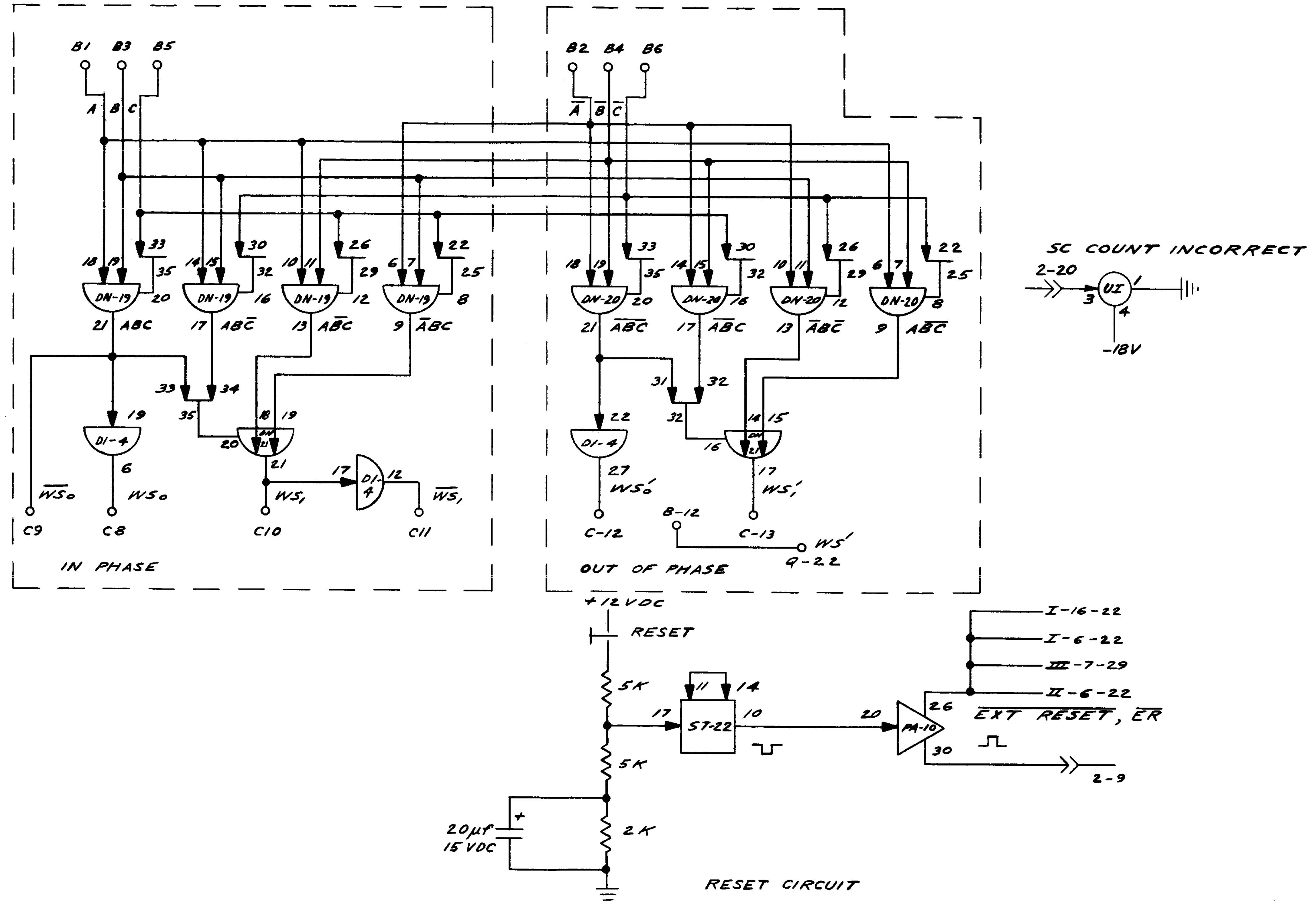


Figure III-5. In-Phase Frame Sync Circuit



NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.

Figure III-6. Word Sync Recognizer

NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.

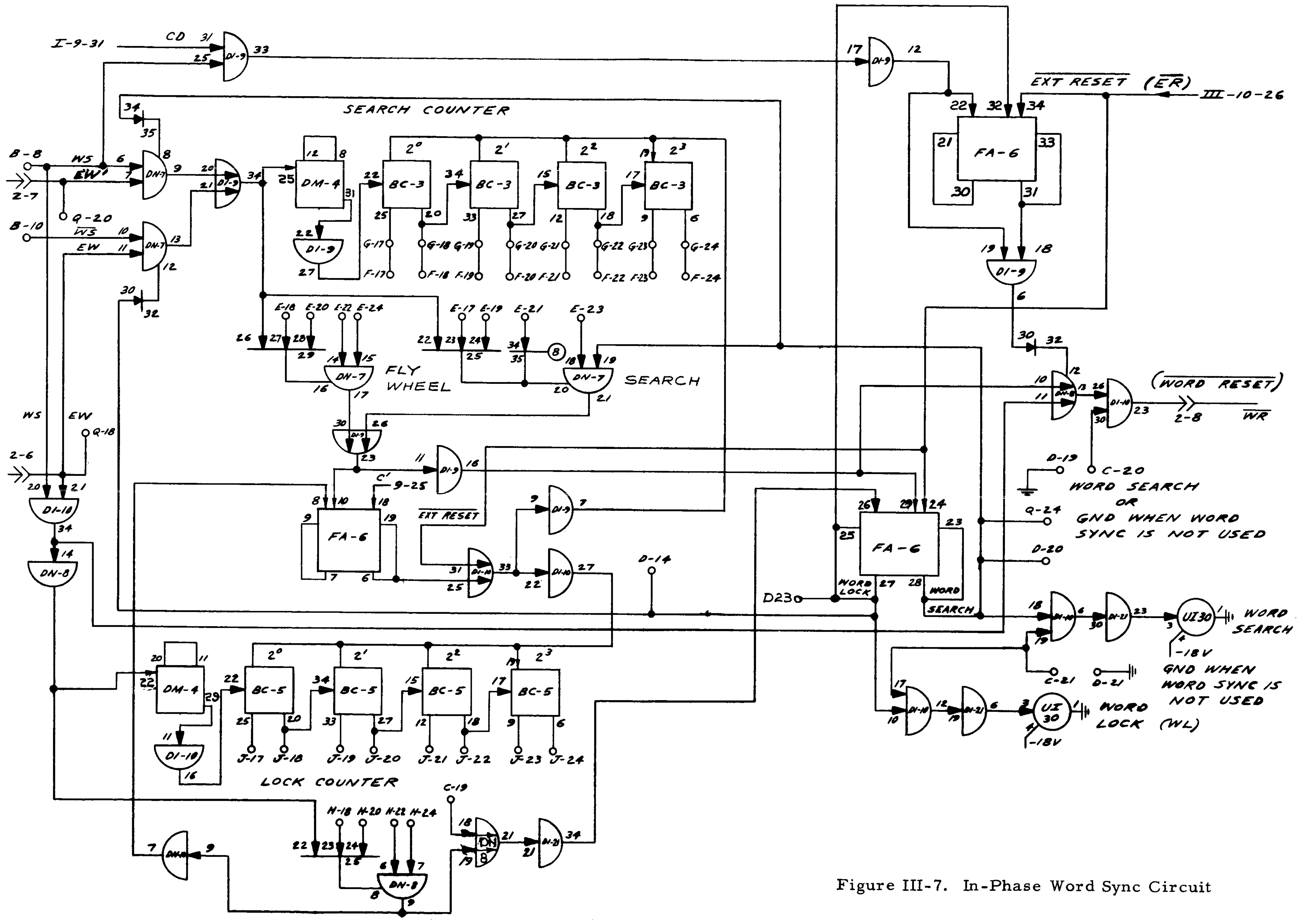
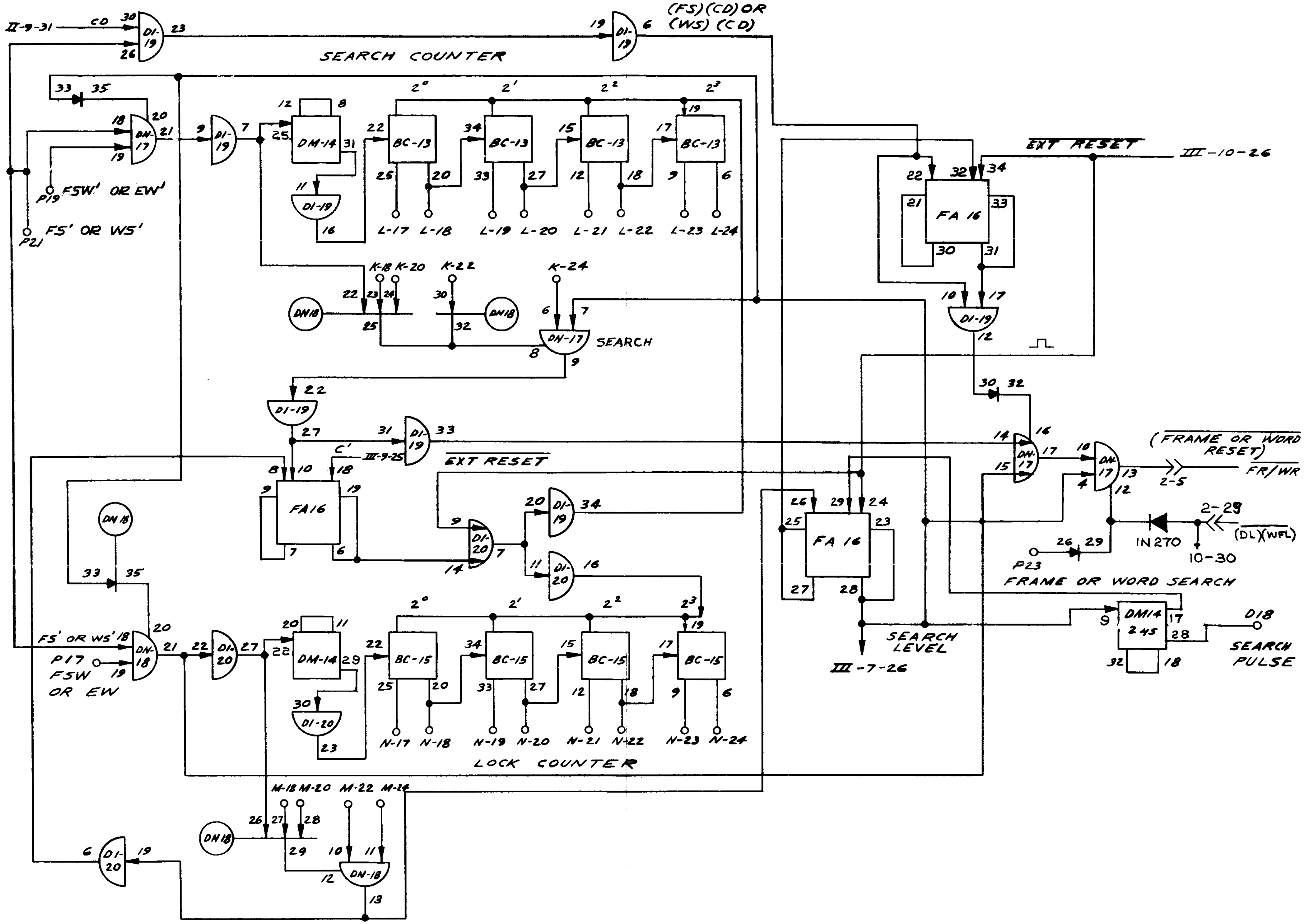


Figure III-7. In-Phase Word Sync Circuit



NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.

Figure III-8. Out-of-Phase Frame Sync Circuit

C. BITS/WORD/FRAME COUNTERS UNIT

FUNCTIONAL DESCRIPTION

The bits/word/frame counters unit supplies FSW and EW pulses necessary to acquire and maintain frame and word sync to the search and lock unit, and acquires and maintains subcom sync. To do this the unit determines and identifies the occurrence of end of words, end of frames, particular main frame words, particular subcom words, and recognizes subcom sync patterns. It consists of nine discrete circuits: a bits/word counter, a words/frame counter, three frames/subcom counters, three subcom sync pattern recognizers, and a subcom counter corrector.

The unit is designed to perform two distinct types of subcom synchronization; one is the detection of a specific sync pattern, the other is making a natural count of main frames located in a specific word(s). In the first case, the fixed sync pattern is recognized and checked for proper location in the main frame. This is an assynchronous subcom used, for example, by the S-17 satellite. In this case subcom sync acquisition requires a subcom pattern recognizer used in conjunction with a frames/subcom counter.

For the second type of subcom synchronization, the word in which the subcom counter is located is checked every frame for a predetermined count of main frames indicating the beginning or end of the subcom. This is a synchronous subcom and is used, for example, by the S-49 satellite. Subcom synchronization in this case requires using a frames/subcom counter in conjunction with the subcom counter corrector circuit.

THEORY OF OPERATION

Bits/Word Counter

The bits/word counter is used to determine the end of words. Figure III-9 is the logic diagram for this circuit. Since the input data is processed through the Data Processor in NRZ there will not be a pulse for every data bit. For this reason $\overline{C}'$ pulses are counted to determine end of word.

The outputs of the counter stages are patched to NAND gate DN6 depending on the number of bits per word for the satellite whose data is being processed. Until end of word occurs, EW' is generated at D17-6. When end of word does occur, these pulses are cut off. At this time EWL is passed through NOR gate DN6-13 to set FA10. The output of FA10 then resets the counter. The counter may also be reset by $\overline{WR}$ or $\overline{WR/FR}$ pulses from the search counters in the search and lock unit as they perform their function.

A word advance pulse is obtained each time FA10 goes to the set condition.

This pulse is used to advance the words/frame counter.

Words/Frame Counter

Word advance pulses are counted in the words/frame counter to obtain FSW, EFP, and frame advance pulses. In addition, any particular word (or words) in a frame can be obtained at the output of the counter stages. Figure III-10 is the logic diagram for this circuit.

For each word advance from the bits/word counter, a positive transition occurs at DI9-6. The positive transitions are counted to give the word count. Inputs to the counter reset gate (patch points W1 through W7) are patched to the output of the counter stages so that the gate will be enabled when the number of words in a frame have been counted. When this gate is enabled EFP is generated at PA16-26. On the trailing edge of EFP, FA10-34 goes positive, putting the FA in the set condition. The outputs of the FA then reset the counter. A frame advance pulse is obtained at FA10-31 each time the flip-flop goes to the set condition.

FSW is obtained by patching the counter preset gate inputs (patch points W8 through W14) to the outputs of the proper counter stages to enable the gate when the frame sync word occurs. (If the frame sync pattern is longer than a single word, the gate is enabled when the last word of the pattern occurs.) At this time FSW will be generated at DI9-12 and its complement, $\overline{FSW}$, at DI9-27. Except for the time FSW is present, FSW' pulses are continuously generated at DI9-33.

Note that the Data Processor must be in sync with the input data if the FSW pulse obtained is in fact in coincidence with the frame sync word. Therefore, before system sync is obtained, the counter is preset by $\overline{FR}$ or $\overline{W/FR}$ from the search and lock counters, or by $\overline{FSW}$, to the word number following the last frame sync word. Thus if the last frame sync word is word number three of each frame, the counter is preset to a count of four. This is the count the counter should contain if the FS or FSW pulses which were obtained are correct. By presetting the word/frame counter the acquisition of system sync is speeded up, so that a minimum of data will be lost.

To preset the counter, patch points U1 through U7 are connected to the proper counter dc set and reset inputs, patch points V1 through V14, so that when DI9-16 goes positive the counter will be set to the desired count. The diodes in series with the reset node input of each counter stage are necessary because this input does not have a built-in buffering diode.

Subcom Sync Acquisition - Fixed Subcom Word Pattern

To obtain subcom sync when the subcom word patterns are fixed it is normally necessary to detect the pattern in the proper subcom word. In some cases, the subcom word is followed by a verification word which must also be recognized in the proper subcom word. After a fixed number of subcom words have been counted, the verification word should then be detected in a second pattern recognizer. If the verification pattern appears in the proper subcom word, a pulse is then generated indicating the acquisition of subcom sync.

Logic diagrams for the three subcom sync recognizers are figures III-11, III-12, and III-13. They differ from the frame sync recognizers only in that a NAND gate is available with the subcom sync pulse and WFL as inputs. A positive output pulse is required in this case. For the operation of the subcom sync pattern recognizer, see the discussion of the frame sync recognizer, paragraph on Search and Lock Function.

The three frames/subcom counters differ in that counter no. 1 has seven counter stages, and counters no. 2 and no. 3 have six counter stages each. Logic diagrams for the three are figures III-14, III-15 and III-16. For this discussion reference is made to figure III-14, frames/subcom counter no. 1.

Using frames/subcom counter no. 1 in this application, the subcom word recognizer is patched to point S13 and the verification word recognizer is patched to point P16. The recognizers should be patched so that S13 goes negative and P16 goes positive when the words are recognized. Counter preset gate inputs (patch points S1 through S8) are patched to the words/frame counter so that the gate is enabled each time a subcom word occurs in a frame of data. (That is, the subcom words for this particular subcom. The satellite may have more than one subcom. For these subcoms other unique words in the main frame will be subcom words.) Patch point N16 goes to the "one" level each time a subcom word is detected, so this point is patched to the counter input, P14. Thus the counter advances each time a subcom word is detected.

Counter preset patch points P1 through P7 are connected to the counter preset inputs Q1 through Q14, so that when FA10-31 goes to the "one" level the counter will preset to the desired count. The outputs of the counter stages are patched to the inputs of the counter auxiliary gate (patch points S9 through S12, and R9, R10, and R11) so that the gate will be enabled when the number of subcom words by which the verification word follows the subcom word pattern have been counted. The output of this gate at R13 is patched to G16. The counter reset gate is also patched to the output of the counter stages so that the counter will reset at this time.

The sequence of operations is as follows: When the subcom word pattern is recognized DI16-7 goes positive. At the same time the words/frame counter should be at the subcom word so that DN9-9 will go positive. If both these actions occur simultaneously FA10-31 goes to the "one" level and the counter is preset (usually to a count of one). Now each time a subcom word occurs in the words/frame counter FA24-31 goes negative and the counter advances by a count of one. The first subcom word was also counter in the same manner.

After the number of subcom words by which the verification word follows the subcom sync word have been counted, DN9-21 goes negative which results in a positive transition at FA24-26. Coincident with this, the verification word should be recognized in a pattern recognizer so that FA24-25 will be at the "zero" level. With this point at the "zero" level, the positive transition at the reset input (pin 26) will put the flip-flop in the reset condition. FA24-28 now goes to the "zero" level which results in a flag being generated in the accumulator to indicate the acquisition of subcom sync.

Subcom Sync Acquisition - Variable Content Subcom Word

When the satellite whose data is being processed uses a particular subcom sync word whose content increases by a count of one each frame, then repeats itself after reaching a maximum count, a frames/subcom counter is used with the subcom counter corrector circuit to acquire and maintain subcom sync.

In this application there is only one subcom word per frame, and it is the same word every frame. The frames/subcom counter is advanced by a count of one each frame by EFP obtained from the words/frame counter. The content of the counter is compared in the subcom counter corrector with the content of the subcom word obtained from the main shift register. As long as there is a one-to-one correspondence between the content of the subcom word and the frames/subcom counter the system is in subcom sync with the data.

In operation, as long as the content of the counter corresponds with the content of the subcom word nothing further occurs in the frames/subcom counter. Should a preselected number of bad comparisons occur in succession, the counter reset gates in the counter corrector will dump the subcom word from the shift register into the counter preset inputs. With the counter now updated to correspond to the content of the subcom word, the correspondence should be maintained for succeeding frames. If not, the counter will be again updated from the shift register after the selected consecutive number of bad comparisons again occurs.

The frames/subcom counter preset gate (fig. III-14) is patched to the output of the words/frame counter (fig. III-10) so that the gate is enabled each time the subcom word appears. The pulse from the gate is used in the subcom counter corrector (fig. III-17). It is obtained at patch point S14 and connected to C34 in the corrector. Both the set and reset outputs of each counter stage are connected to the comparison circuit gates in the corrector. The counter preset inputs (patch points Q1 through Q14) are connected to the counter reset gates, also in the corrector. If the counter is to count less than 128 frames (its capacity), then the counter reset gate must be patched into the outputs of the counter stages so that the counter will reset when the highest frame number occurs.

The input to the corrector is a comparator circuit for checking the content of the frames/subcom counter. Both the set and reset outputs of each counter and shift register are patched to the input gates of the comparator. Patch points E21 through E34 receive the outputs of the counter stages, and patch points F21 through F34 receive the outputs of the main shift register stages. Since there are 14 input gates, the length of the subcom word is limited to seven bits.

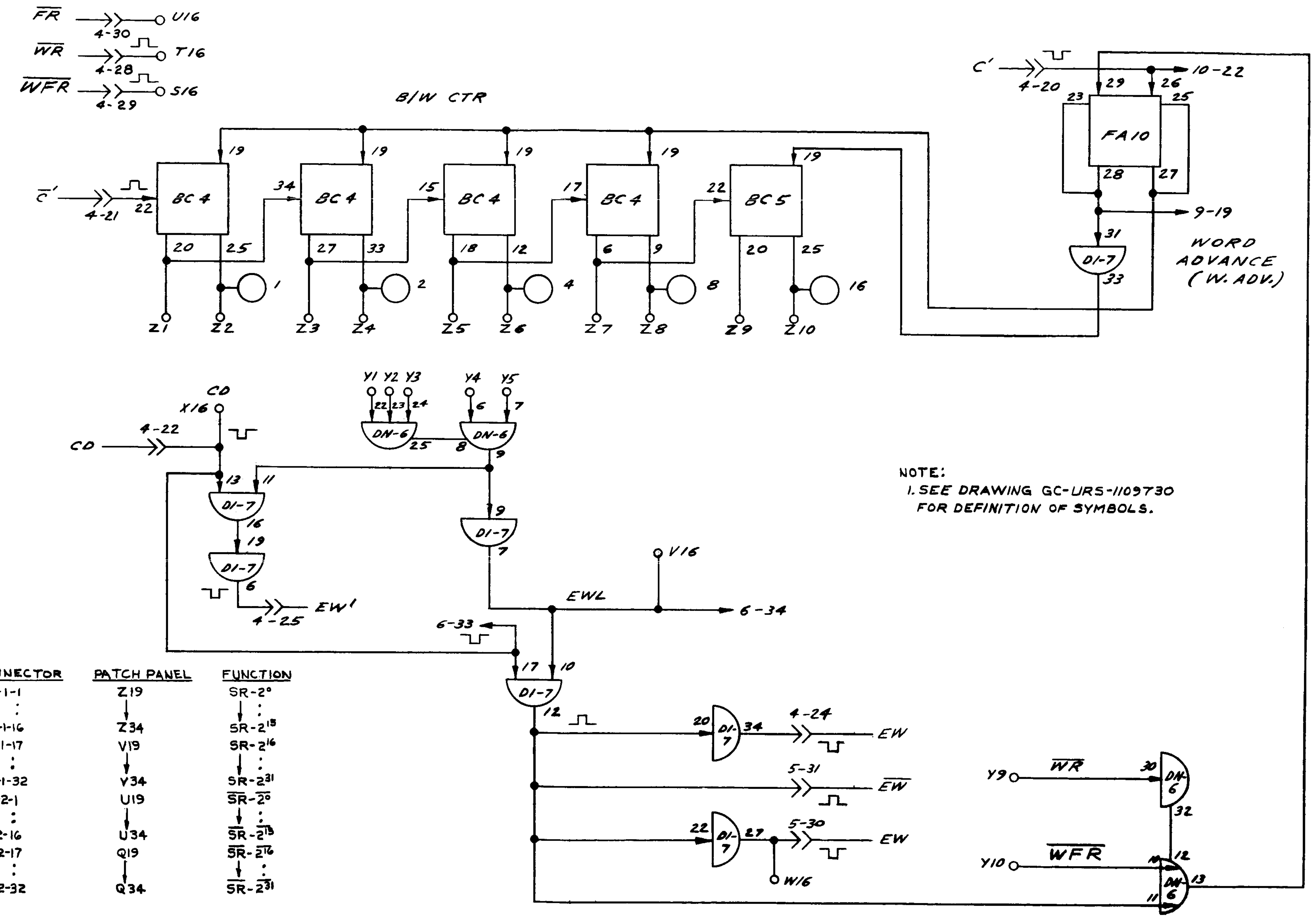
A four-stage counter is used to count bad comparisons. The output of the counter is patched so a strobe pulse will be generated to dump the subcom sync word from the shift register into the frames/subcom counter after a selected number of consecutive bad comparisons have occurred. This number may be two to eight. After eight consecutive bad comparisons the SUBFRAME COUNT INCORRECT indicator located on the search and lock unit lights to warn the operator that subcom sync has been lost.

The content of the subcom word in the shift register is available at the series of NAND gates attached to patch points D21 through D34. These gates are used to update the frames/subcom counter to agree with the subcom word. Patch points D21 through D27 are connected to the set inputs of the counter, and D28 through D34 are connected to the reset inputs. The gates are strobed after the preselected number of consecutive bad comparisons have occurred.

Comparisons are continually being made in the comparator circuit since it is patched into the main shift register. However, the only comparison of interest is the one which occurs when the subcom sync word is in the comparator input gates. Therefore, the output of the comparator is strobed by a negative pulse obtained from patch point S14 of the frames/subcom counter when the subcom word occurs. This pulse is connected to patch point C34.

The output of the comparator circuit, DN24-21, is at the "zero" level for a good comparison, and at the "one" level for a bad comparison. If the comparison was good, DN24-9 goes positive when the subcom word strobe pulse arrives, and the counter is reset. If the comparison was bad, DN24-17 goes positive and DI23-23 goes negative when the subcom word strobe pulse arrives. This results in advancing the counter by a count of one, and a positive transition at FA10-15. The positive transition has no effect on the flip-flop, as its reset level control (pin 16) is not at the "zero" level. Should the preselected consecutive number of bad comparisons occur for which the output of the counter is patched, FA10-16 will go positive. If the next comparison is bad, the positive transition at FA10-15 will result in the flip-flop going to the reset condition. This results in strobe pulses at DI23-12 and DI23-16 which update the frames/subcom counter to match the content of the subcom word. FA10 remains in the reset state until the next subcom word pulse is received or the system reset pushbutton is depressed.

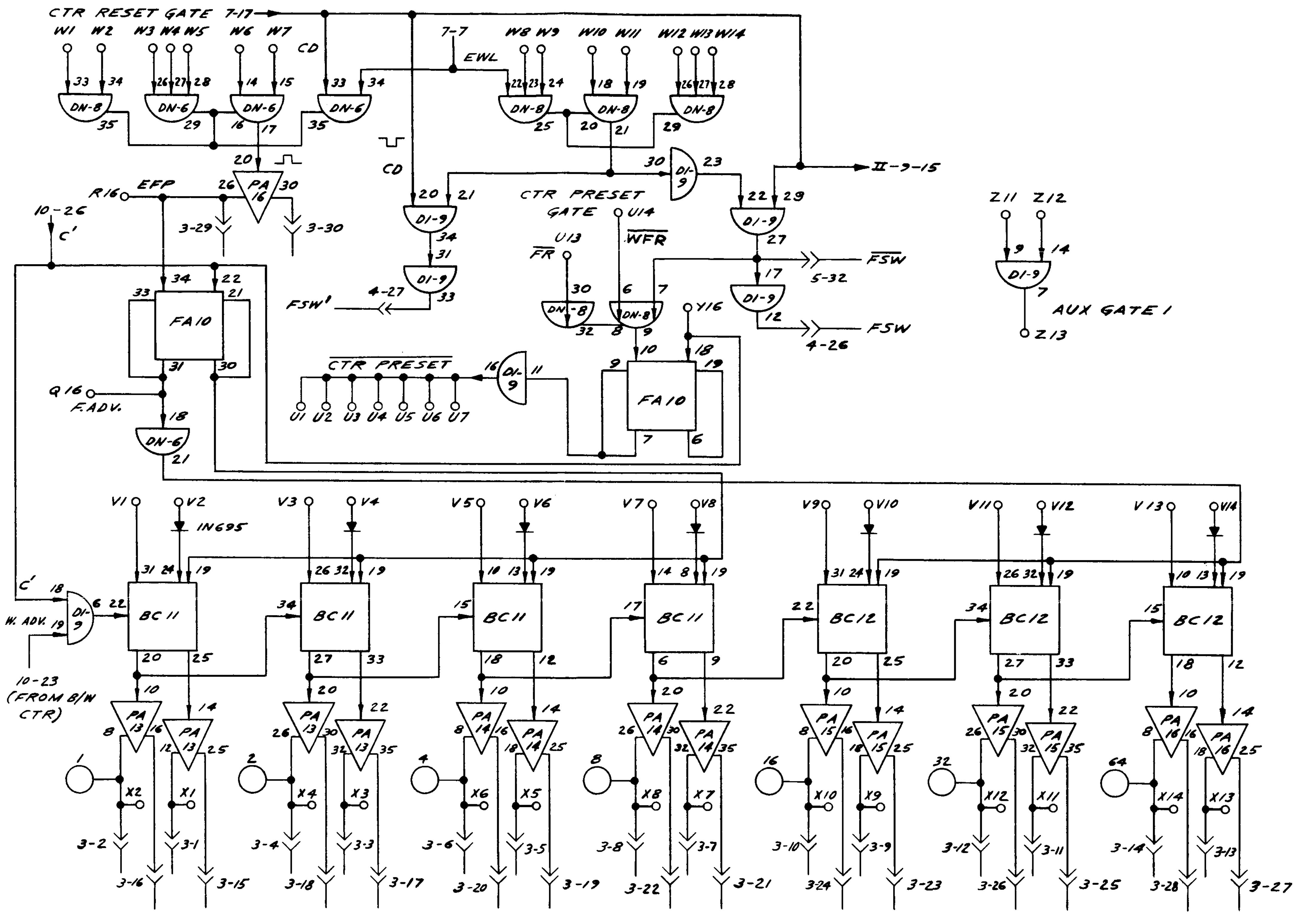
If eight consecutive bad comparisons occur BC25-9 goes to the positive condition. This enables the attached NOR gate so that DI23-6 goes negative. The SUBFRAME COUNT INCORRECT indicator then lights.



CONNECTOR	PATCH PANEL	FUNCTION
B-1-1	Z19	SR-2°
↓ :	↓	↓ :
B-1-16	Z34	SR-2¹⁵
B-1-17	V19	SR-2¹⁶
↓ :	↓	↓ :
B-1-32	Y34	SR-2³¹
B-2-1	U19	$\overline{SR}$-2°
↓ :	↓	↓ :
B-2-16	U34	$\overline{SR}$-2¹⁵
B-2-17	Q19	$\overline{SR}$-2¹⁶
↓ :	↓	↓ :
B-2-32	Q34	$\overline{SR}$-2³¹

PATCH PANEL PINS WIRED TO GROUND: C17 THRU Z17

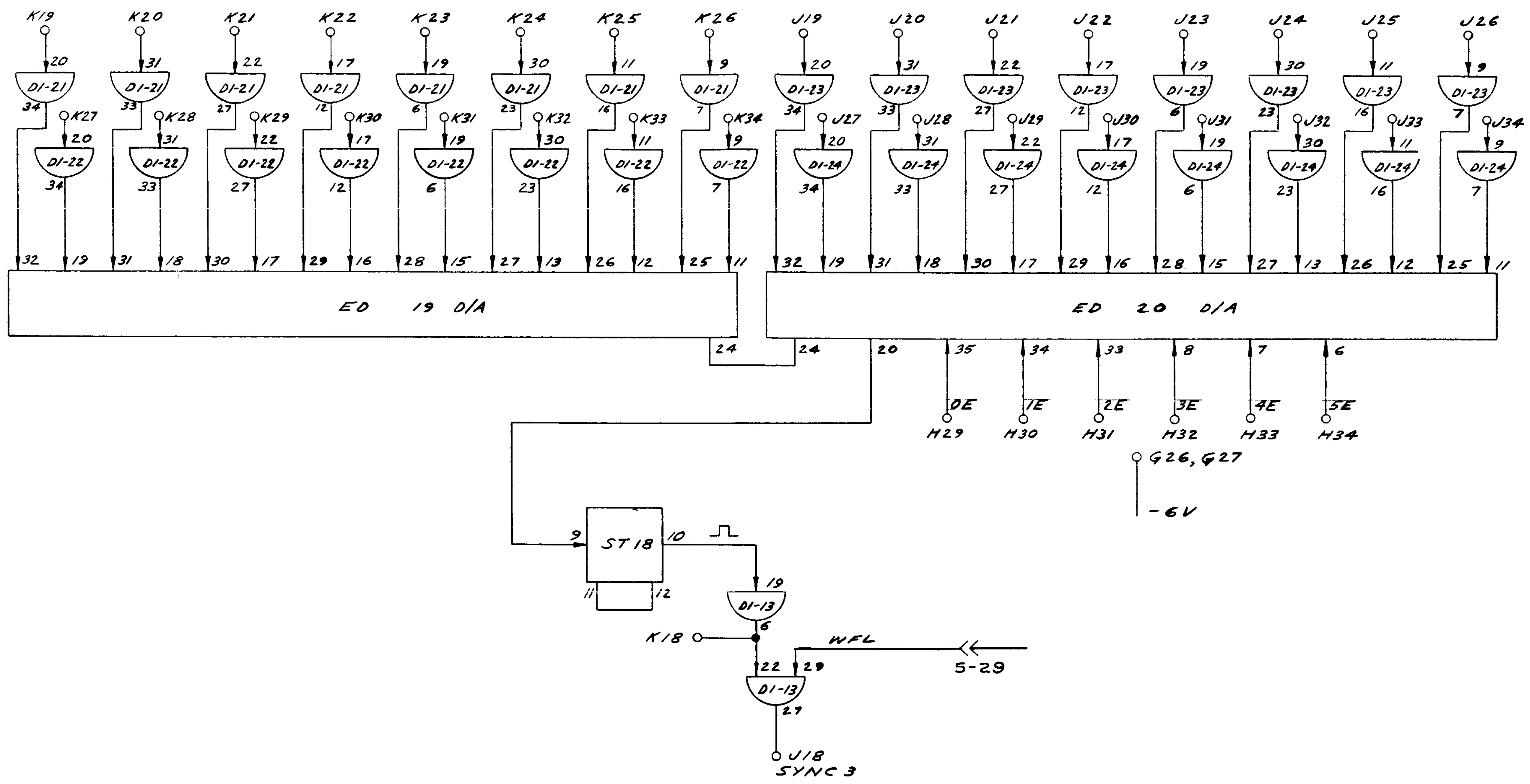
Figure III-9. Bits/Word Counter



WORDS/FRAME COUNTER (W/F CTR)

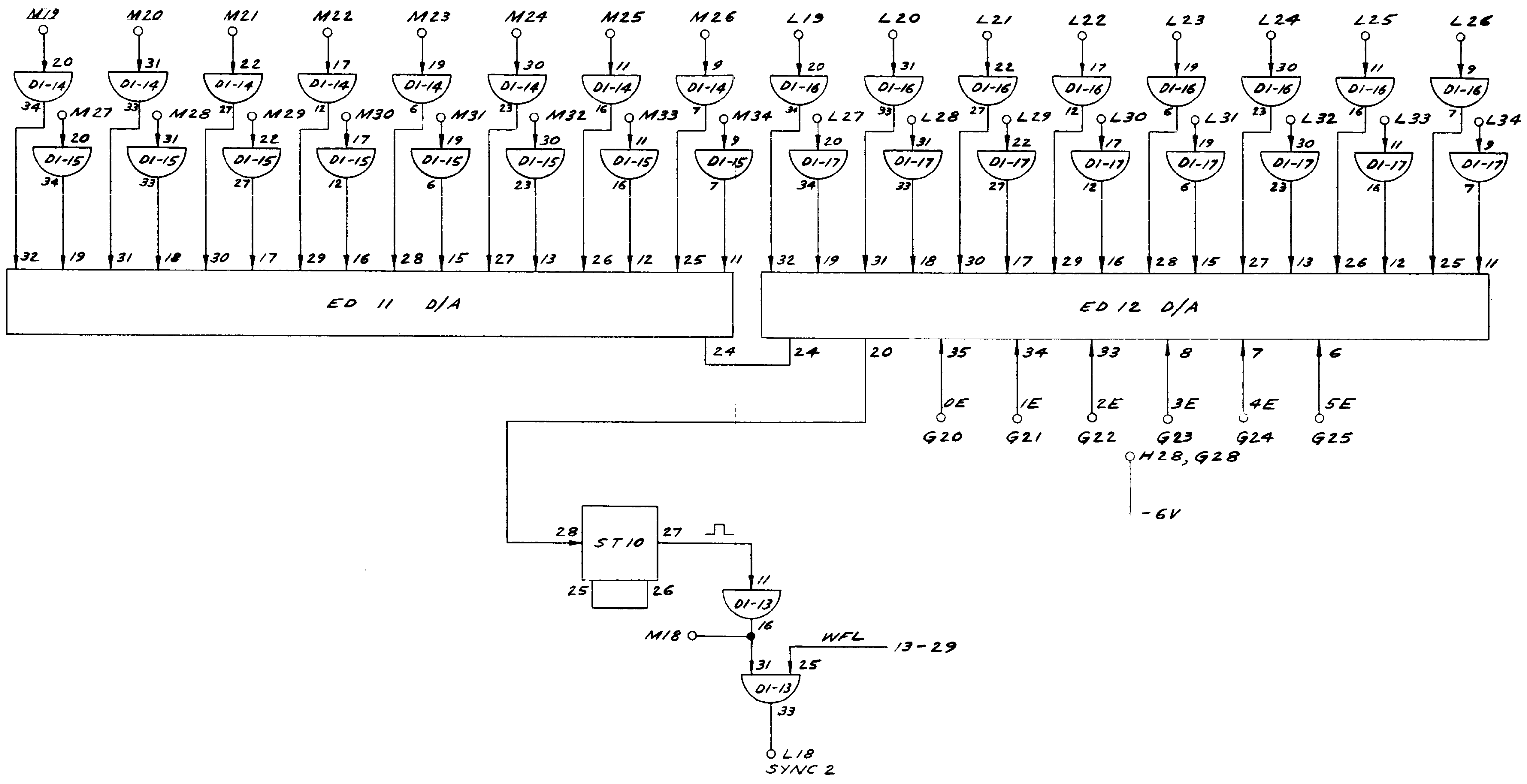
NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.

Figure III-10. Words/Frame Counter



NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.
2. GATE INPUTS NOT PATCHED TO S.R. OUTPUTS SHALL BE PATCHED TO GROUND (SEE DWG. 1109747

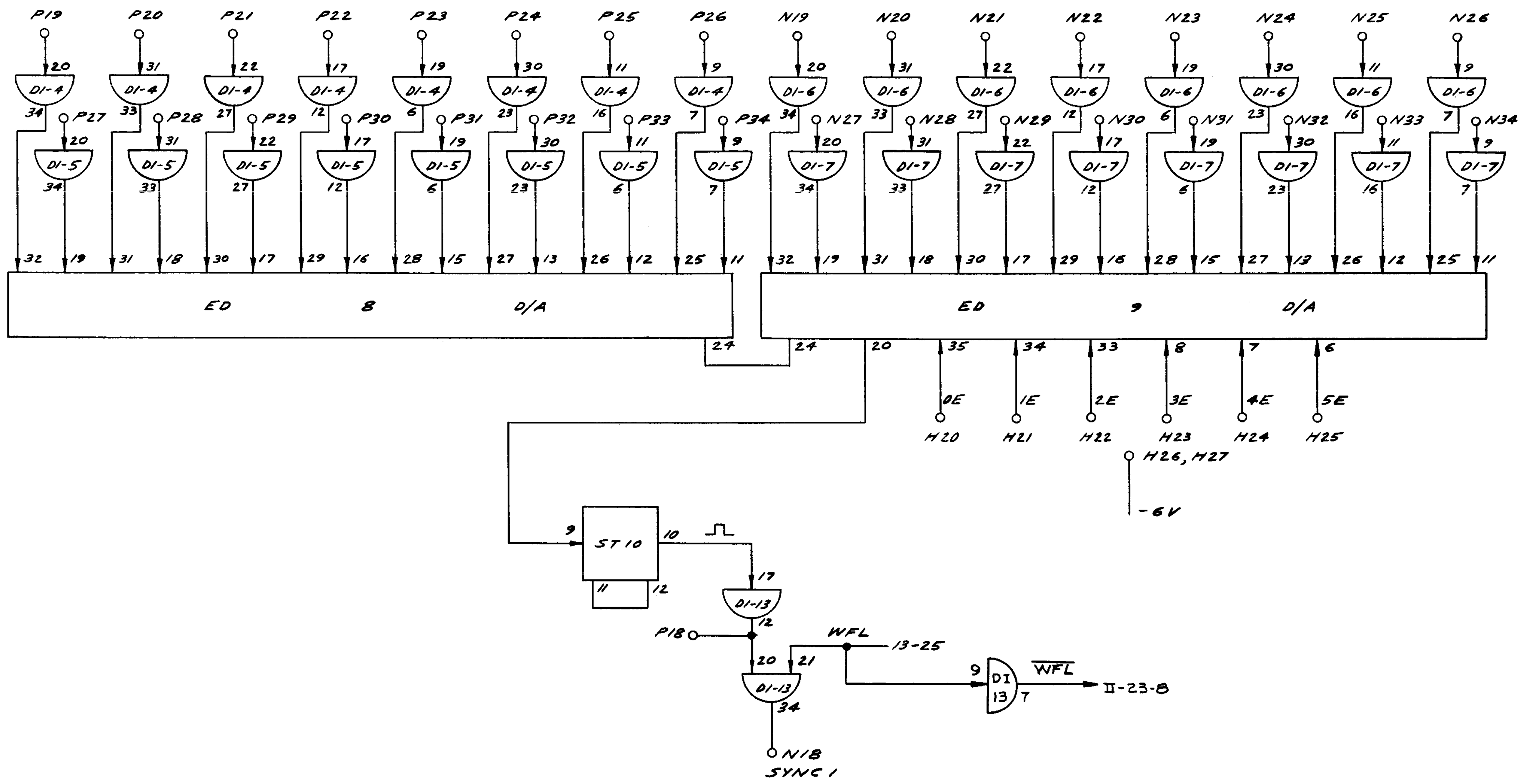
Figure III-11. Subcom Sync Recognizer 3



NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.

2. GATE INPUTS NOT PATCHED TO S.R. OUTPUTS SHALL BE PATCHED TO GROUND (SEE DWG. 1109747).

Figure III-12. Subcom Sync Recognizer 2



NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.
2. GATE INPUTS NOT PATCHED TO S.R. OUTPUTS SHALL BE PATCHED TO GROUND (SEE DWG. 1109747).

Figure III-13. Subcom Sync Recognizer 1

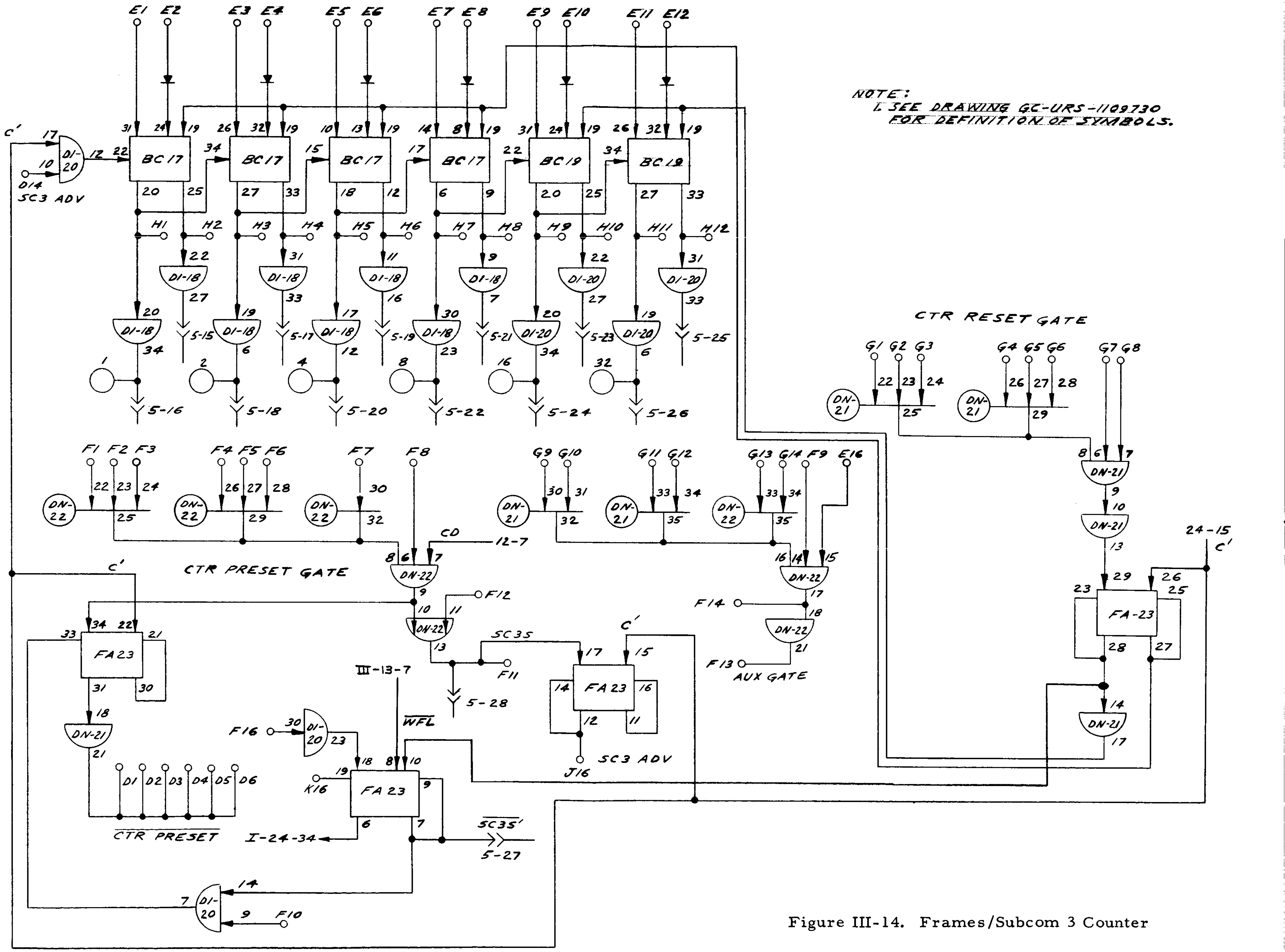


Figure III-14. Frames/Subcom 3 Counter

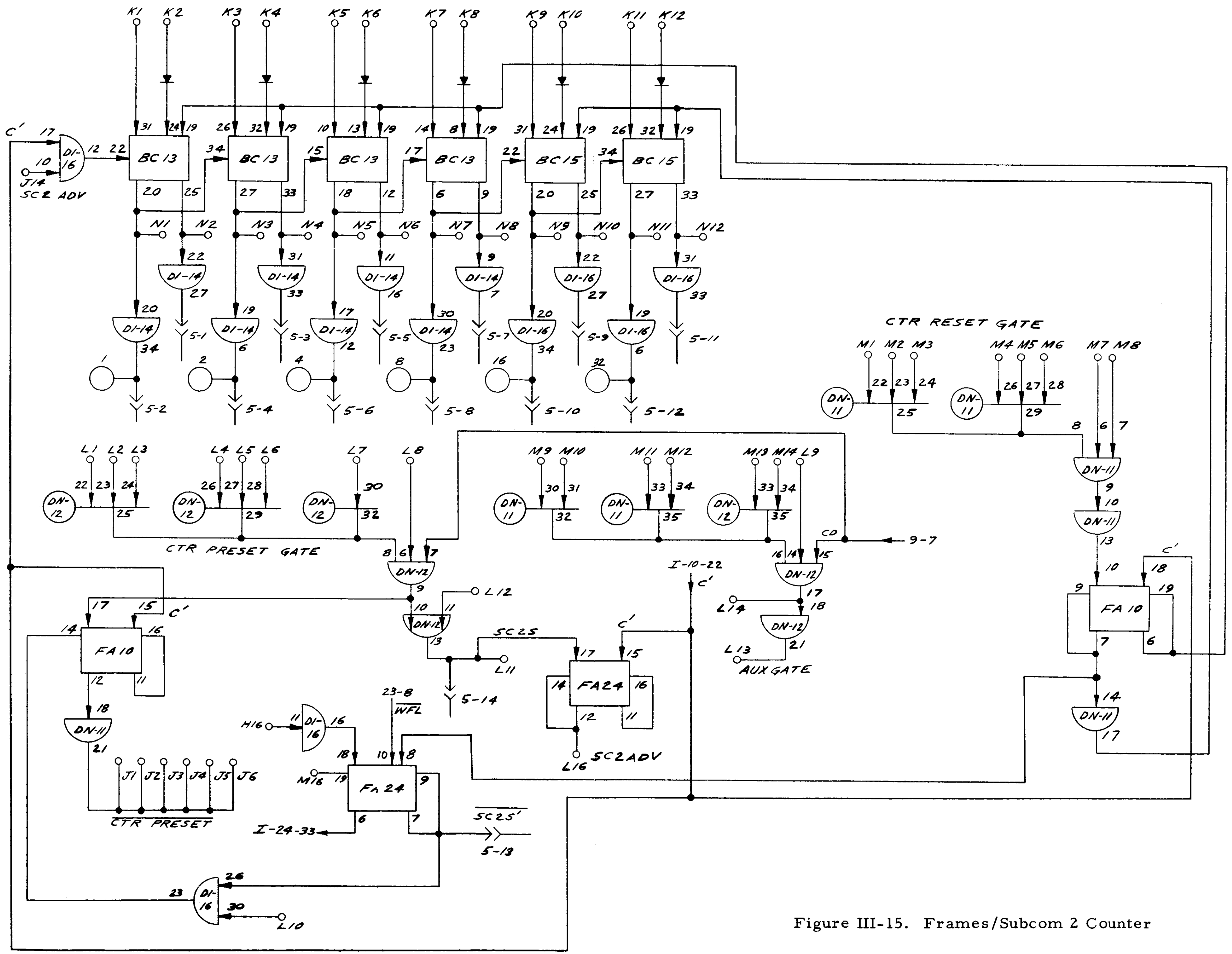


Figure III-15. Frames/Subcom 2 Counter

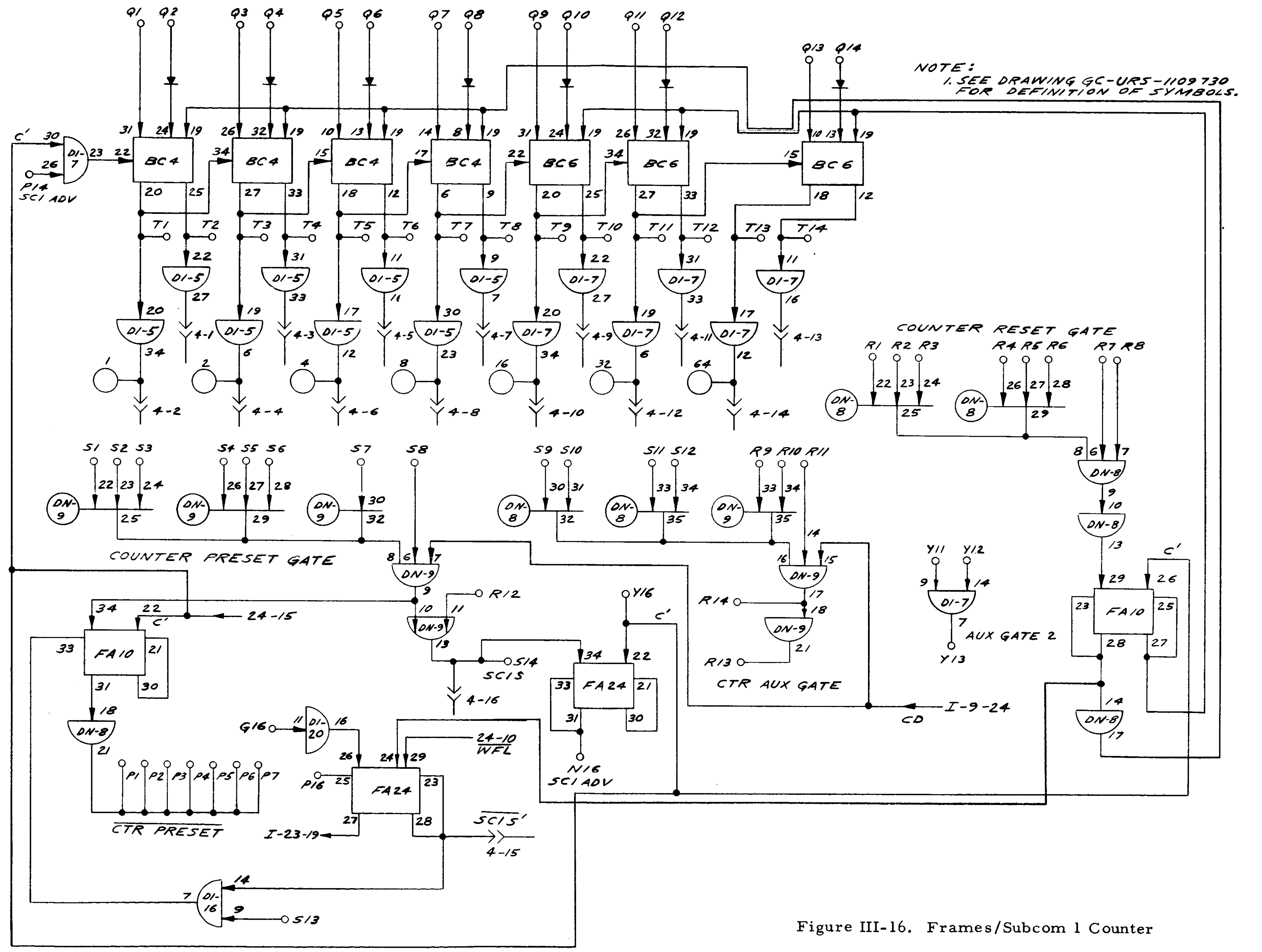


Figure III-16. Frames/Subcom 1 Counter

NOTE: SEE DRAWING GC-URS-1109730
FOR DEFINITION OF SYMBOLS.

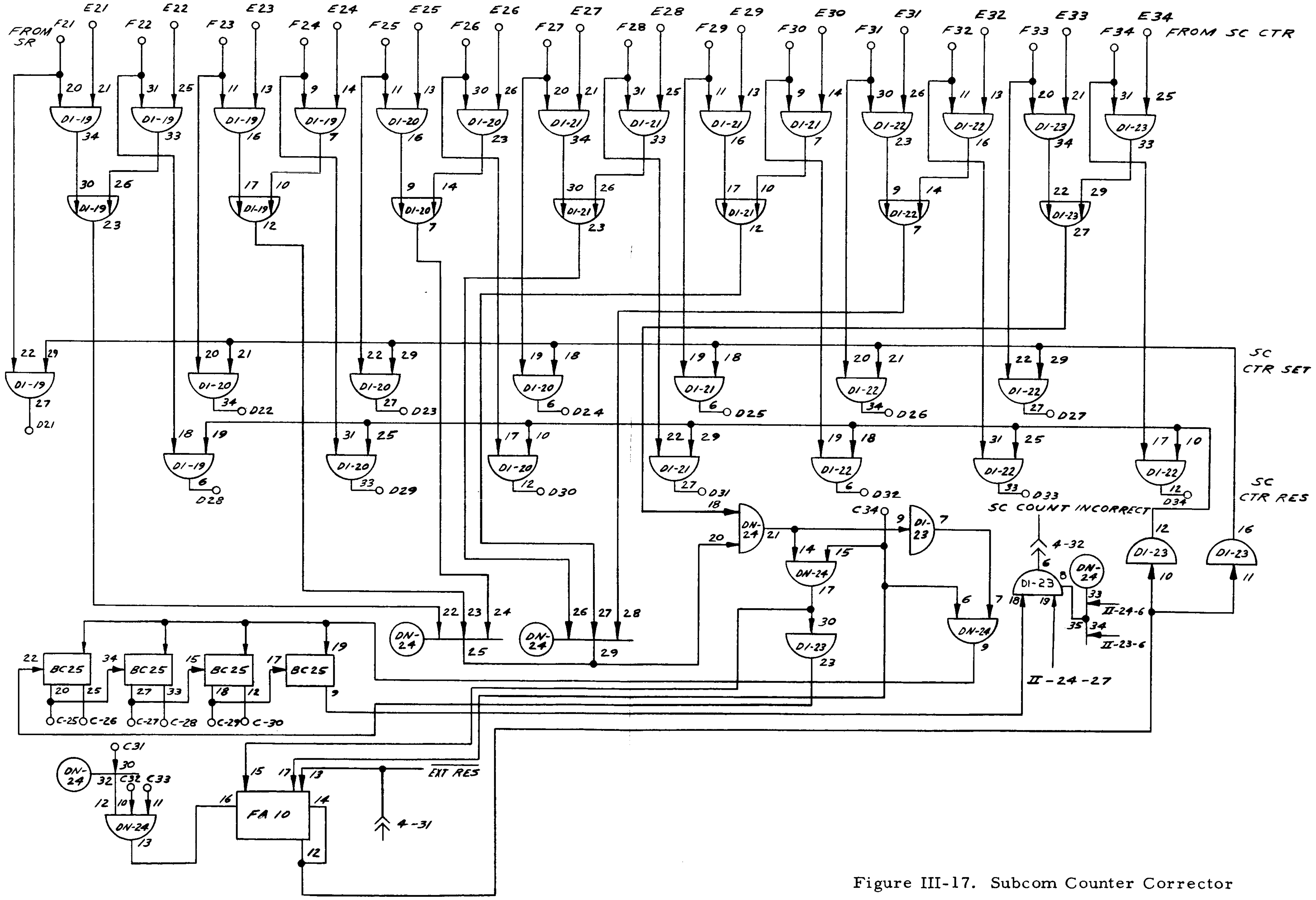


Figure III-17. Subcom Counter Corrector

D. ACCUMULATOR UNIT

FUNCTIONAL DESCRIPTION

The accumulator is an extremely versatile unit consisting of unrelated counters, gates, flip-flops, one-shots, and indicators which may be connected by patching. Its operation largely depends on the format requirements of the satellite whose data is being processed. Certain common commands are required by the buffer regardless of the satellite format, but the method of generating these commands in the accumulator will likely be different for each satellite.

Functions performed by the accumulator are:

(1) Generates commands for the buffer. These include data present (DP), time present (TP), subcom sync (SCS), dump, a special (or alternate) DP, and frame sync quality. DP, TP, and dump will always be required. Which of the others are used depends on the requirements of the particular satellite. All buffer commands are positive 2-usec pulses.

(2) Provides data to the buffer in a specified format and at specific time intervals. Data is strobed from the data register of the accumulator by the buffer following each DP pulse. The data register can accommodate up to 32 bits; the first nine bit positions (2^0 to 2^8) of the register may be multiplexed to provide the frame sync bit error count and the content of subcom no. 1 counter on the regular data lines.

(3) Generates special flags such as subcom present, subcom location in main frame of data, and frame sync quality (or confidence).

(4) Detects a change in bit rate of the input data, and sounds a buzzer to alert the operator. A flag is also sent to the buffer at this time indicating change of bit rate. The operator must then adjust the synchronizer to the new bit rate in order to reacquire frame sync. Bit rate change detection circuitry is included to meet a special requirement of the S-17 satellite.

In the theory of operation discussion which follows the operation of the accumulator will be related to its actual use with the S-17 and S-49 satellites. The unit functions in a different manner for each of these satellites, therefore, the reader should get a better idea of how the accumulator may be used to accommodate other satellites with different formats.

Buffer Commands

The accumulator can generate a maximum of six commands for the buffer. These include DP, TP, SCS, dump, alternate DP, and frame sync quality. In figure III-18, the gate and indicator marked flag 1 is used to send alternate DP to buffer and indicate that it has been generated. Likewise, flag 2 is used for SCS, flag 3 for dump, and flag 4 for frame sync quality. Probably every command will not be needed for a particular satellite, so those not needed are not generated. All commands are initiated at the end of specific words or at end of frame. However, due to buffer timing, all commands are delayed before being sent to the buffer. SCS and dump are always generated at end of frame. If, for example, frame sync is lost, the dump command is automatically generated, but not until end of frame so that the frame being processed when sync was lost will be passed to the buffer before processing stops. All commands are inhibited by the buffer when it is not able to accept data.

Data present commands instruct the buffer to strobe data being held in the accumulator data register. If the buffer is able to accept data at this time it does so. Data is also strobed into the accumulator data register each time DP is generated. For the S-49 satellite, a DP pulse is generated every three words; for the S-17, at the end of every two words.

EW pulses are counted to obtain DP for S-49. The pulses are counted by binary counter BC20 (fig. III-19) whose output is decoded by NAND gate DN19. Each time three EW pulses are counted a DP pulse is obtained at patch point G14. BC20 is reset at this time by DMA27 whose output is patched to H14. The one-shot is triggered by NOR gate $\overline{\text{DP}}$ and EF pulses obtained from gate 3 (fig. III-18). The output from gate three is also patched to D1 (fig. III-20) where it is used to strobe data into the accumulator data register. From G14, the DP pulse is patched to DMA25 (fig. III-18). DMA25 provides a 60-usec delay, and then triggers DM12 (fig. III-21). The output pulse from DM12 ($\overline{\text{DP}}'$) is taken from J12 and patched to E12 of gate 2 and D11 of the frame sync quality flip-flop FA13 (fig. III-18). $\overline{\text{DP}}$ is gated with $\overline{\text{EF}}$ in gate 2. The output from gate 2 is taken at E14 and gated with (WFL)(DL) in gate 4. (WFL)(DL) is gated with all commands so that if frame sync is lost, commands cannot be sent to the buffer. (It is obtained at patch point B1, figure III-20). The output of gate 4 is patched to K15 to trigger DMA26 which provides the DP command for the buffer.

For the S-17 satellite a DP pulse is required at the end of every two words. Therefore, EW, (WFL)(DL), and the 2^0 bit from the words/frame counter are gated together at DN10 (fig. III-20) to obtain DP. The output of the gate is taken at J17 and patched to DMA25 (fig. III-18). DMA25 provides a 60-usec delay, and then triggers DMA26 whose output pulse is the buffer DP command. The DP output pulse from NAND gate DN10 also strobe data into the accumulator data register.

The time present command instructs the buffer to strobe time from the time decoder. For the S-49, TP is initiated at the end of each frame, and sent to the buffer after an 80-usec delay. For the S-17, the command is initiated at the end of word 1 of each frame, and sent to the buffer after the same delay. EF and (WFL)(DL) are patched to the time present gate (fig. III-18) for S-49. The output of the gate is patched to J2 where it triggers DMA27. After a 80-usec delay, the output pulse from DMA27-10 is sent to the buffer as the time present command. The command for S-17 is generated in the same manner except that word 1 from the words/frame counter is patched into the time present gate along with EW and (WFL)(DL).

The subcom sync command instructs the buffer to start writing records at a specific frame. It is generated at end of frame and transmitted to the buffer after a delay.

For the S-49, gate 1 (fig. III-18) is patched into the output of subcom counter no. 1 so that the gate is enabled on a count of 127. The output of the gate is patched to J7, the level control on FA23 (fig. III-19). EF is patched to the reset input of the flip-flop (J8) so that it goes to the reset conditions with the arrival of the first EF pulse after gate 1 is enabled. The output of FA23 (J5) is patched to J6, the input of NAND gate DI22. The other inputs to the DI are EF and (WFL)(DL). DMA26-25 is triggered by the gate output, and provides a 240-usec delay. Patch points J9 and J4 are connected so that the output at DMA26-31 triggers DMA26-22. The output of this DMA, B3, is patched to the flag 2 input gate (fig. III-18) along with WFL and (WFL)(DL). Each time the gate is enabled a subcom sync command is sent to the buffer.

For the S-17 satellite, every other subcom sync command generated is sent to the buffer. This is done by placing a flip-flop to perform a divide-by-two function between the DMA which provides the necessary delay and the output DMA.

To generate the subcom sync command for this satellite, $\overline{SC1S'}$ is patched to the level control (J7) of FA23 (fig. III-19). Gate 1 (fig. III-18) is patched to subcom counter no. 1 so that it is enabled by word 47 or 48 of subcom 1. The output of the gate is patched to the reset input (J8) of FA23, thus the flip-flop goes to the reset condition when word 47 or 48 of subcom 1 occurs, provided subcom 1 sync has been acquired. The reset output at FA23-6 is patched to J6, one input of DI22. The other inputs of the DI are connected to EF and (WFL)(DL) so that DMA26-25 is triggered when end of frame occurs. The output of the one-shot is wired to FA23-13 and -15, the set and reset inputs of the flip-flop, so that FA23-11 is at the "one" level for alternate subcom sync pulses. The output of the flip-flop (J3) is patched to J4, one input to NAND gate DI22. (WFL)(DL) is patched to the other gate input (K3). Each time FA23-11 goes to the "one" level there is a 2-usec pulse from DMA26-10. This pulse, along with WFL, is patched to the input of the flag 2 gate. Each time the gate is enabled a subcom sync command pulse is sent to the buffer.

A dump command is generated whenever frame sync is lost. It is initiated at end of frame and sent to the buffer after a 240-usec delay. The dump circuit functions identically for both the S-49 and S-17 satellites. $\overline{(WFL)(DL)}$ is permanently connected to DI22-19 (fig. III-19). If frame sync is lost, $\overline{(WFL)(DL)}$ goes negative, and triggers the attached DMA which, after a 240-usec delay, triggers DMA25-22. The output from the latter DMA (B2) is patched to the input gate for flag 3 where it is inverted and passed on to the buffer.

The S-49 satellites generate a frame sync quality command which instructs the buffer to generate a frame sync quality flag. This command is generated at the end of each frame so long as the frame sync bit errors do not exceed a predetermined number. The set level control of the frame sync quality flip-flop (fig. III-18) is permanently connected to the frame sync error indicator in the error monitor unit. As long as the set number of bit errors does not occur the level control remains at the "zero" level. The set input of the FA (C15) is patched to CD; the set output (B20) is patched to the flag 4 input gate along with EF. As long as frame sync quality is good the command is sent to the buffer at end of frame. If the quality goes bad, FA13-33 goes to the "one" level and the command cannot be generated. The flip-flop is returned to the reset condition each frame by patching $\overline{DP'}$ to D11.

Data Register and Output Circuits

The accumulator data register receives the output of the main shift register from the shift register output power amplifiers located in the error monitor unit, and passes it to the buffer in a specific format and at specified time intervals. The output of each stage of the register is passed through a NAND gate or a DI inverter which isolates the accumulator from the input circuits of the buffer. The first nine bit positions (2^0 through 2^8) of the register may be multiplexed with the content of the frame sync bit error counter and subcom counter no. 1, so that this information may be sent to the buffer on regular data lines when desired.

Up to 32 bits can be accommodated by the data register (fig. III-20). If the last five stages of the register are used (2^{27} through 2^{31}), their outputs must be patched to the DI inverters identified by indicator triodes number 28 through 32 shown in figure III-21. Indicator triodes 19 through 22 (fig. III-20) may be shared, therefore, if they are to be used with the data register they must be patched to register stages 2^{18} through 2^{21}. Note that the reset output of the 2^0 through 2^8 register stages are used, whereas the set outputs of the 2^9 through 2^{31} stages are used. This is because the outputs of the 2^0 through 2^8 stages are used as inputs to NAND gates; the remaining stages are merely passed through DI inverters to the buffer.

Input data is fed to the level control inputs of each FA of the data register. An FA will go to the set or reset condition when strobed depending on whether the set or reset level control is at the "zero" level when the strobe pulse arrives. The number of bits dumped into the data register and sent to the buffer is dependent on how often DP pulses are generated. The S-17 word consists of eight bits; the S-49 word consists of nine bits. Since a DP pulse is generated at the end of every other word for the S-17, sixteen bits are strobed into the register for each DP pulse. For the S-49 a DP pulse is generated every three words, so that 27 bits are strobed into the register for each DP pulse.

Strobe pulses for the register are obtained by patching into patch points D1 and K17. Gated EW pulses and 2^0 pulses from the words/frame counter are used as strobe pulses for the S-17. The output of the gate at patch point J17 is also used as the DP pulse for this satellite. Strobe pulses for the S-49 are obtained by patching $\overline{(DP)}(EF)$ pulses to point D1.

Data cannot be strobed into the register until WFL is obtained, or if WFL is lost after the system is in sync. The buffer also prevents strobing data into the register when it is not ready to receive it by inhibiting DI11-13. WFL is patched to point G17. When the system acquires sync FA9-14 goes to the "zero" level, so that the first EF pulse (patched to H17) causes the flip-flop to go to the set condition. The strobe gate is now enabled and data can be strobed into the register. If WFL is lost, or if the data sync inhibit line from the buffer goes positive, FA9-16 goes positive and the next EF pulse causes the flip-flop to go to the reset condition, inhibiting the strobe gate.

The output of the flip-flop at patch point B1 is also used to control command gates so that commands cannot be sent to the buffer if the flip-flop is in the reset condition. (WFL)(DL) is obtained at this point. This flip-flop is also controlled by the DATA PRESENT-DATA DELETE switch, SW1. With the switch in the DATA DELETE position, FA9-16 goes to the positive level so that the next EF pulse puts the flip-flop in the reset condition. Thus data cannot enter the register, nor can commands be sent to the buffer.

The buffer output circuits (fig. III-21) receive the output of the data register and makes it available to the buffer. When required, the contents of the frame sync bit error counter and subcom counter no. 1 can also be transferred through this circuit to the buffer. The 2^0 through 2^8 bits from the data register are fed to NAND gates controlled by the output at FA13-27. The 2^9 through 2^{31} bits from the register are passed through DI inverters and on to the buffer. When the 2^{27} through 2^{31} bits are required, they must be patched to the DI inverters identified by triode indicators no. 28 through 32. These same inverters may also be used to send special flags to the buffer.

If the contents of the frame sync bit error counter and subcom counter no. 1 are to be sent to the buffer, FA13-28 must be at the "zero" level. For the S-49 satellite this is done by patching EF to K5. This enables the gates attached to the frame sync bit error counter and to subcom counter no. 1, and inhibits the gates attached to the 2^0 through 2^8 stages of the data register. FA13-28 is returned to the "one" level by the first DP pulse of the frame so that data can be passed through the gates to the buffer. This circuit is not used for the S-17. For this satellite, EF pulses are patched to K6 to ensure that the data gates remain enabled.

Special Flags

Special flags are sent to the buffer to indicate such things as subcom present, subcom locations in the main frame, end of file, and frame sync quality. The flip-flops identified as auxiliary flags and indicators in figure III-18 may be used for this purpose, as well as any available gates in the figure. Flags may be sent to the buffer over regular data lines by patching into K9 through K12, J15 and J16, or A20 (see fig. III-21). The frame sync quality flip-flop and two of the auxiliary flag flip-flops (FA14-12 and FA15-28) are permanently connected to output lines.

Only one flag (subcom sync) is generated for the S-49 satellite, whereas ten flags are generated for the S-17. For the latter satellite, the occurrence of the three subcom syncs, particular words in each subcom, and two frames of all "ones" are flagged, as are change of bit rate and frame sync quality. Four examples will be discussed here: three are rather routine, and the fourth, "two frames of all ones" for the S-17, requires the use of flip-flops included in the accumulator specifically for this purpose. The change of bit rate flag will be discussed in paragraph on Bit Rate Change Detector in connection with the special circuit used to detect change of bit rate.

The subcom sync flag for the S-49 is obtained at the time the subcom sync command is initiated. The subcom sync flag pulse is taken at patch point J5 (fig. III-19) passed through an inverter, and sent to the buffer by patching the inverter output to K10 (fig. III-21). Subcom no. 1 of the S-17 is flagged by patching $\overline{SC1S'}$ to the set level control (D14) of FA13, and the 2^5 bit from subcom no. 1 counter to the set input (D12) of the FA (fig. III-18). The output of the flip-flop (D15) is sent to the buffer by patching to K11 (fig. III-21). EF is patched to D13 to return the flip-flop to the reset condition. Word 2 of subcom no. 1 is flagged by patching the output of the subcom no. 1 flag flip-flop (D15) to the set input (C12) of FA14. $\overline{2^4}$ from the words/frame counter is patched to the set level control (C11) of the flip-flop. Thus if subcom 1 sync occurs while $\overline{2^4}$ is at the "zero" level, the flag which is generated indicates that subcom no. 1 occurred in word 2 of the main frame. The flag is sent to the buffer by patching the flip-flop output (C14) to J16 (see fig. III-21). This flip-flop is also returned to the reset condition by patching EF to the reset input.

To generate the flag indicating two frames of all "ones" for the S-17, the two four-stage counters shown in figure III-19 are used in conjunction with the two FA15 flip-flops shown on the same figure. The two counters are connected by patching H12 to H13 and H14 to H15 to form a single eight-stage counter. A frame of all "ones" gives a count of 192, therefore, the counter output gate is patched into the counter to decode this count. Input to the counter is the 2^0 bit from the main shift register obtained at patch point C2 (fig. III-20). The gate output is taken at G13 and patched to H1 and H2, the inputs to the two FA15 flip-flops. When the first count of 192 occurs FA15-12 goes to the "zero" level. The other flip-flop was not affected because its level control, FA15-19, was at the "one" level. Now that this point is at "zero" level, the next count of 192 causes FA15-7 to go to the "zero" level, and a flag is sent to the buffer. J1 is patched to K9 for this purpose. The counter is reset at end of frame.

Bit Rate Change Detector

Data from the S-17 is transmitted at two bit rates. Real time data is sent at 400 cps, and recorded data is sent at 7.2 kc. The first data on an analog tape for one pass of the satellite will be real time at the low bit rate followed by recorded data at the high bit rate. In some cases the bit rate on the tape may go from the high rate back to the low rate. The bit rate change detector circuit sounds a buzzer which alerts the operator that the bit rate has changed. He then must set the synchronizer to the new bit rate so that the Data Processor can reacquire sync. If the data goes from the low bit rate to the high rate, and then back to the low, a stop command is sent to the buffer indicating end of file. The buzzer also sounds in this case. Figure III-21 contains the logic diagram for the bit rate change detector circuit.

The input data is fed through a DI inverter to FIL6, a special circuit card containing four bandpass filters. One filter passes 400 cps and a second passes 7.2 kc. The two remaining filters are tuned to four times these frequencies so that analog tapes may be processed at four times the recorded speed. The output from the filter which will pass the input frequency is fed to SC8. This special circuit card contains an emitter follower for each output from FIL6. The signal from SC8 then triggers a ST. Special circuit cards are discussed in Section V.

The first data on the input tape will be at the low bit rate (400 cps, or four times this if the tape is played back at four times the recorded speed). FA13-31, FA13-6, and FA13-11 are all at the "zero" level as a result of $\overline{\mathrm{ER}}$ pulses when the system is initially started. This places DI11-30 at the "zero" level and the gate is inhibited. The output from DI11-16 cannot pass further, so nothing happens until the bit rate changes from low to high.

When this occurs, there will be an output from ST10-10 or ST10-27, depending on whether or not the input tape is being played at the recorded speed or four times the recorded speed. As a result, a positive transition occurs at DM12-25, triggering the one-shot. B24 is patched to K10 to flag the change of bit rate. The positive pulse from the one-shot places FA13-31 and FA12-11 at the "one" level (K13 is patched to K14). The buzzer now sounds. It is cut off by $\overline{\mathrm{WFL}}$ at FA13-31 when the Data Processor again syncs with the input data at the new bit rate. FA13-31 remains at the "one" level so that if the bit rate returns from high to low, a signal can be gated through DI11-26 to again sound the buzzer alarm and send a stop command to the buffer.

Should this high to low change of bit rate occur, DI11-23 will go positive triggering the one-shot at DM12-26, and putting FA13-7 in the "zero" state. The buzzer now sounds and a stop command is sent to the buffer indicating end of file. Before processing of data can begin again, the synchronizer must be readjusted for the low bit rate and the external reset button must be depressed to reset the three flip-flops in the bit rate change detector circuit.

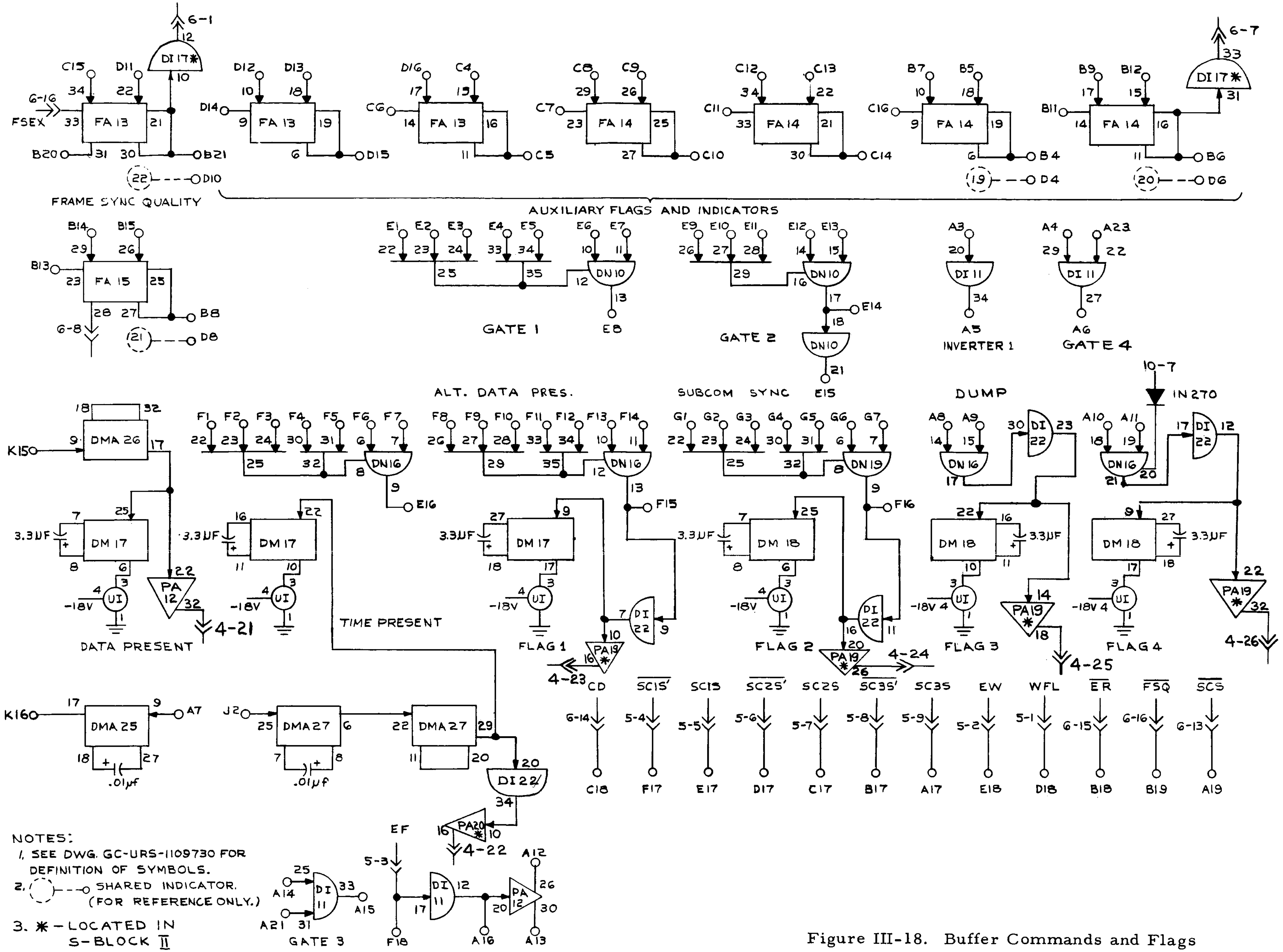


Figure III-18. Buffer Commands and Flags

NOTES:
1. SEE DWG. GC-URS-1109730 FOR DEFINITION OF SYMBOLS

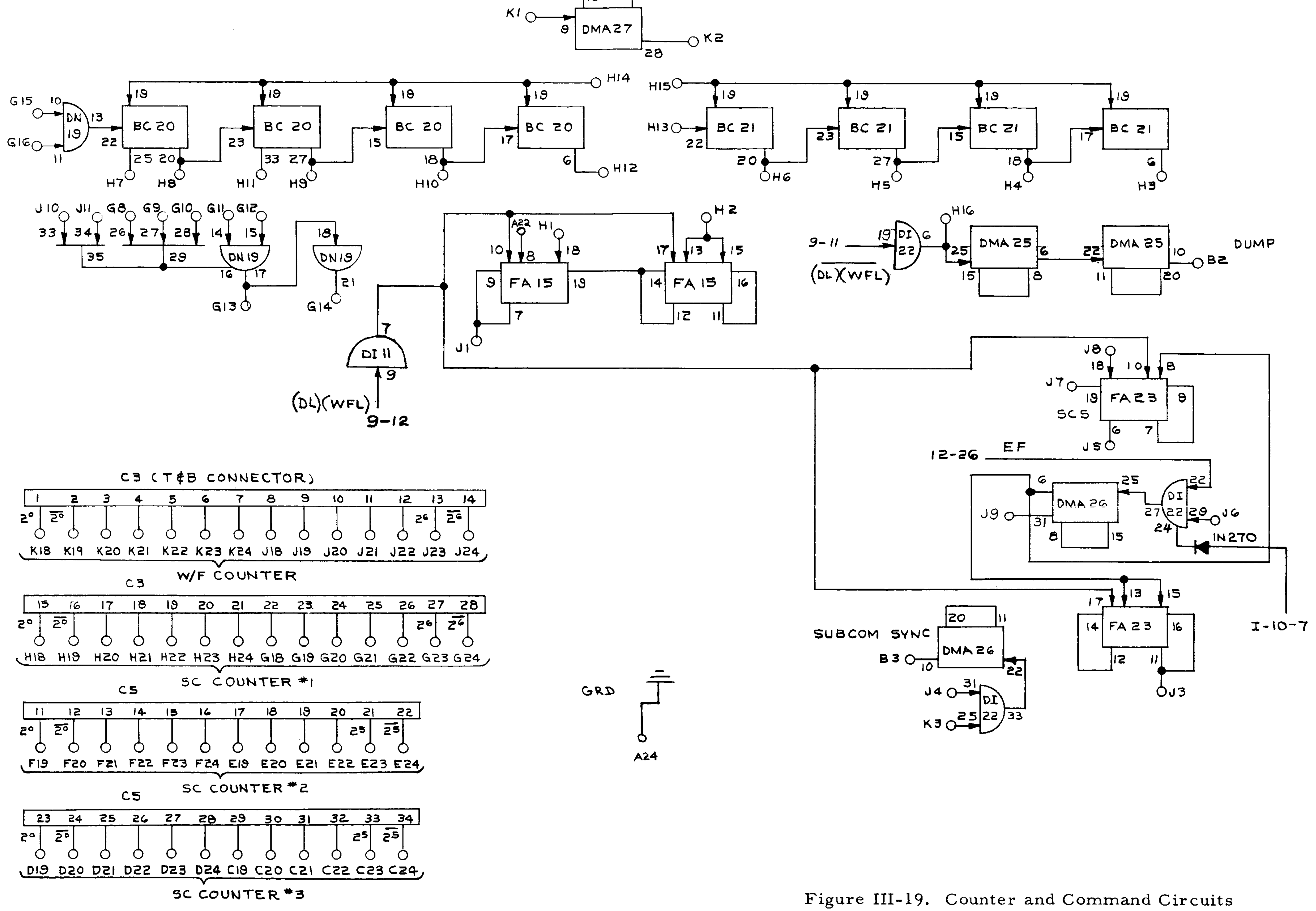


Figure III-19. Counter and Command Circuits

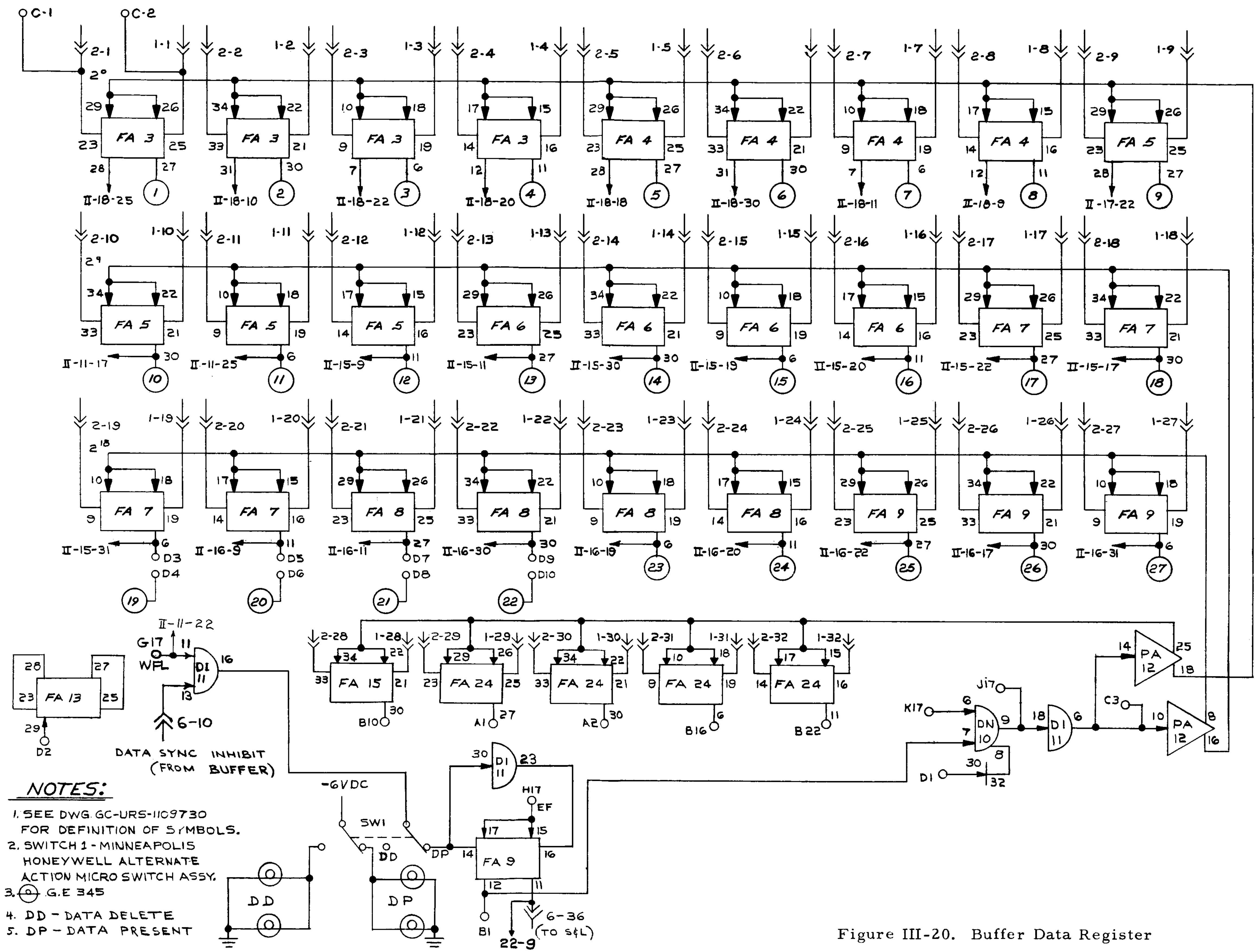


Figure III-20. Buffer Data Register

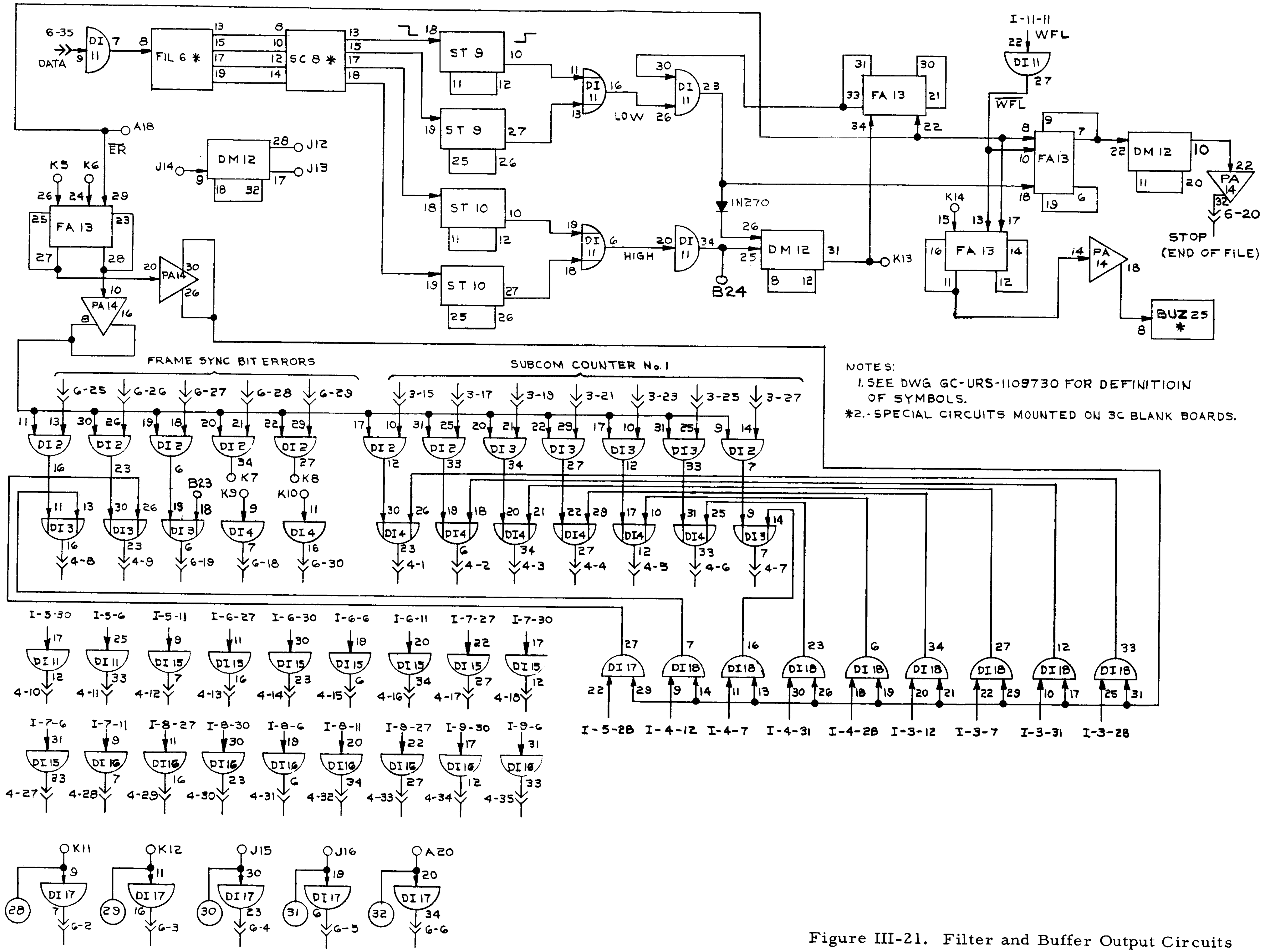


Figure III-21. Filter and Buffer Output Circuits

E. ERROR MONITOR UNIT

FUNCTIONAL DESCRIPTION

The error monitor unit gives a visual indication of frame sync bit errors and parity errors. Signals are also sent to the accumulator so that flags may be generated to indicate the occurrence of a predetermined number of frame sync bit errors. Located in the error monitor unit are the power amplifiers for the main shift register. These amplifiers distribute the input data from the register to the bits/word/frame counters unit, the accumulator unit, and the quick look monitor unit.

THEORY OF OPERATION

Frame Sync Bit Error Monitor

The frame sync bit error monitor is made up of the frame sync bit error register (fig. III-22), the bit error counter and the frame sync error indicator circuit (fig. III-23). The input gates to the shift register are patched to the complements of the frame sync pattern at main shift register output PA's (fig. III-24). If there are no errors in the frame sync pattern the input to each gate used will be a "zero" when the gates are strobed. Errors in the pattern will result in "ones" at gate inputs where errors exist. When the gates are strobed, the gates with "one" inputs will set a "one" (an error) into their attached shift register stages.

$\overline{\text{FSW}}$ pulses (once per frame) are used to strobe the input gates, and thus load all errors ("ones") into the shift register. The pulses are inverted by the PA's driving the strobe lines, so the lines go negative when the pulses occur. $\overline{\text{C}'}$ pulses shift the detected errors through the shift register and into the frame sync bit error counter.

The outputs from the frame sync error shift register (SR14-6, SR14-9) are fed to the set and reset level controls (pins 25 and 23) of FA19 (fig. III-23). Each time a "one" is shifted out of the register to FA19-25 the reset level control at pin 23 will be positive and allow the $\overline{\text{C}'}$ pulse to set FA19-28. The NAND gate at the output of the FA is strobed by a CD pulse which sets a "one" in the five-stage counter.

Shifting and counting of bit errors begins at the end of the frame sync word following the $\overline{\text{FSW}}$ pulse and may take the entire time interval corresponding to all frame sync bits. The frame sync quality level at FA19-11 is therefore established at the end of the last frame sync bit once every frame.

The contents of the counter are continually monitored by indicator triodes connected to the reset output of each counter stage. The set outputs of the counter stages are sent to the accumulator unit. Error selector switch S1 and the NAND gate network at the set output of the first three counter stages permits programming the number of bit errors which must occur before the excessive bit error indicator lights, and a signal is sent to the accumulator to indicate that this has occurred. This latter signal is obtained at FA19-11. It is sent to the accumulator as an indication of frame sync quality.

The counter is reset by each $\overline{\text{FSW}}$ pulse or by the system reset push button. The excessive bit error indicator FA is reset at this time if the AUTO-MANUAL toggle switch is in the AUTO position. If the switch is in the MANUAL position the FA is not reset until the push button switch, S3, is depressed. The excessive bit error indicator glows until this FA is reset.

Parity Error Monitor

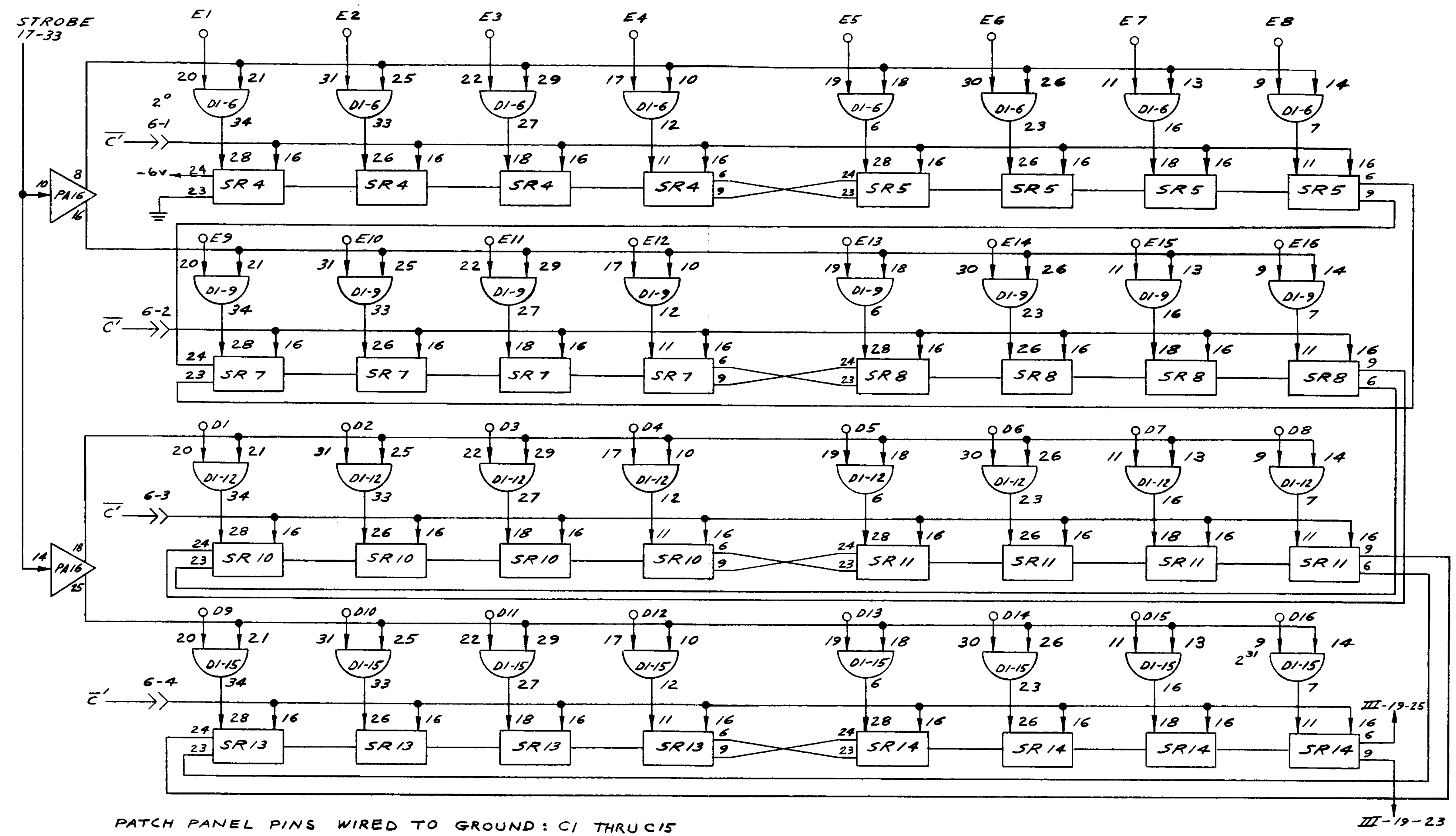
Parity errors may be monitored by connecting patch point J21 (fig. III-23) to the 2^0 position in the main shift register. The bit from the register is gated with CD so that DI20-34 goes positive for every bit which passes through the register. This causes the FA attached to DI20-34 to alternate between the set and reset condition for every "one" bit. If odd parity is being checked the set output (pin 31) will be at the "one" level if there is an error; if even parity is being checked the reset output (pin 30) will be at the "one" level if there is an error. The two NAND gates at the outputs of the FA are strobed by FA19-28 at the end of every word. $\overline{\text{C'}}$ pulse resets FA19-28.

The total number of parity errors is accumulated once per frame. The parity error counter is reset by the EF pulse every frame. It is clear that parity errors are detected only when a parity bit is added to every telemetry word.

Depending on whether odd or even parity is being checked, H21 or H22 is patched to the input of the error counter, J22. Errors are counted until the arrival of the EF pulse which resets the counter. The contents of the counter are monitored by indicator triodes connected to the reset output of each counter stage. Excessive parity errors are indicated by a UI-30 which glows after the number of errors selected by switch S4 have occurred. If the AUTO-MANUAL toggle switch is in the AUTO position, the FA driving the UI-30 is reset with the counter and the indicator is extinguished. If the switch is in the MANUAL position, the indicator glows until the reset push button switch is depressed.

Shift Register Output Power Amplifiers

The shift register output power amplifiers distribute the data in the main shift register (serial-to-parallel converter) through the Data Processor. Figure III-24 is the logic diagram for this circuit. There are two PA's in series for each of the 32 stages of the shift register. Input to the PA's is taken from the set output (true) of each stage. Due to signal inversion in the PA's the output at PA4-16, for example, is the negation of the input signal, and the output at PA4-25 is the assertion of the input signal. Connectors no. 2 and 3 route the data into the bits/word/frame counters unit and the accumulator; connectors no. 4 and 5 route it to the quick look monitor. Note that the assertion outputs are on the odd numbered connectors and the negation outputs are on the even numbered connectors.



PATCH PANEL PINS WIRED TO GROUND: C1 THRU C15

NOTE:

1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.
2. GATE INPUTS ARE PATCHED TO THE COMPLEMENTARY BITS OF THE FRAME SYNC PATTERN.
3. UNUSED INPUTS ARE PATCHED TO GROUND.

Figure III-22. Frame Sync Error Shift Register

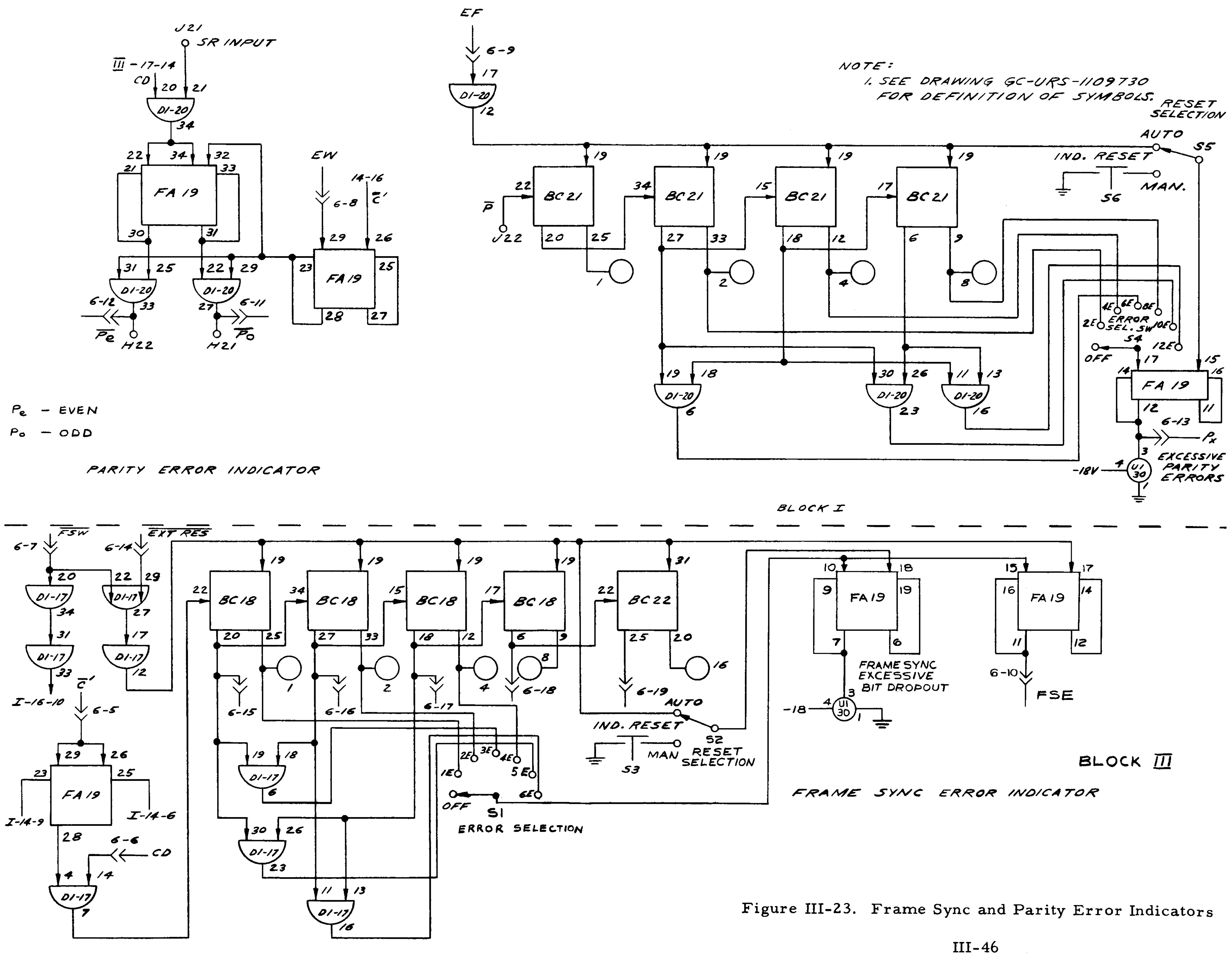
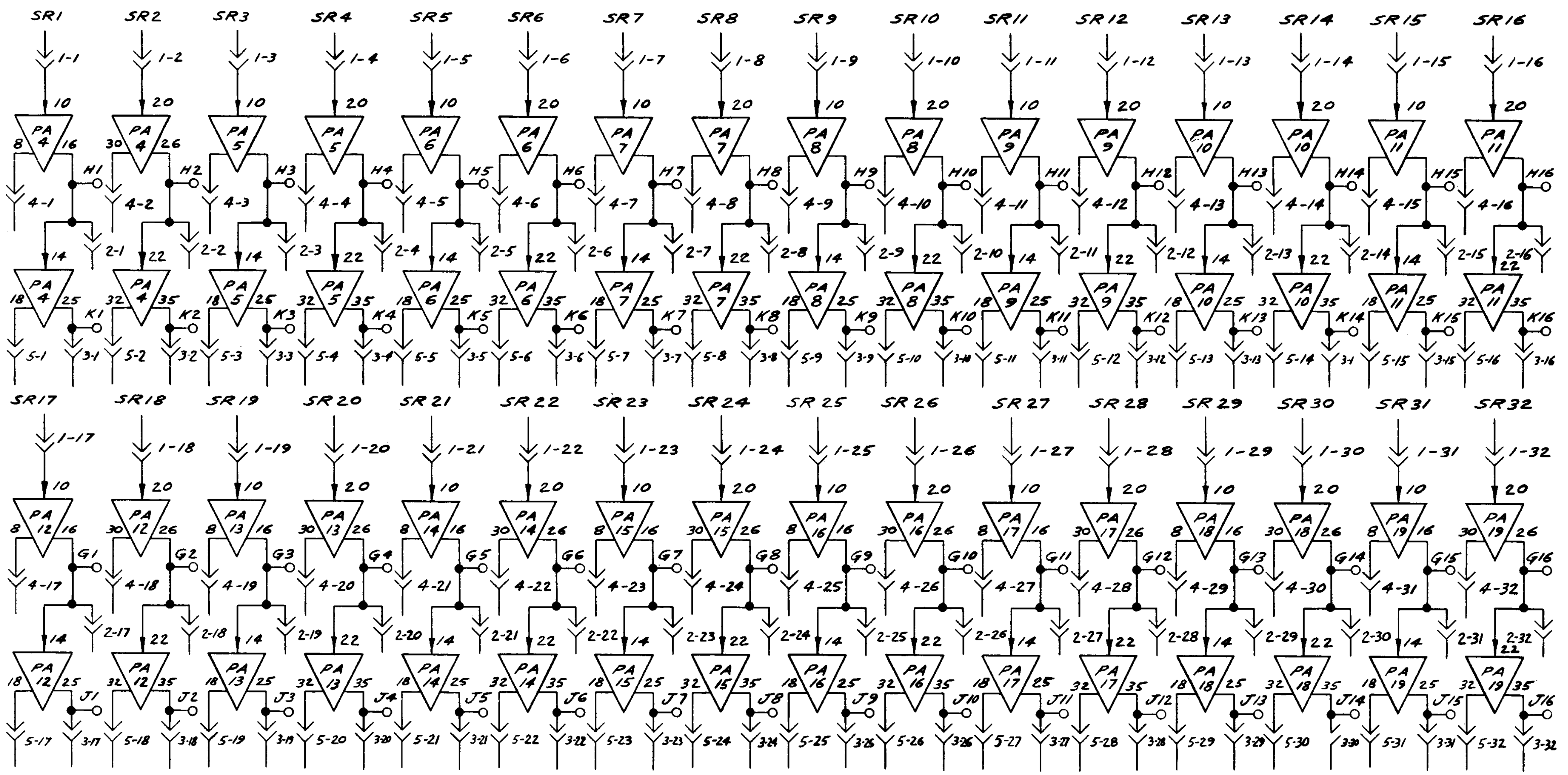


Figure III-23. Frame Sync and Parity Error Indicators



NOTES:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.
2. OUTPUTS OF THESE AMPLIFIERS ARE DISTRIBUTED TO THE QUICK LOOK, ACCUMULATOR, AND B/W/F COUNTERS UNIT.

Figure III-24. Shift Register Output Power Amplifiers

F. QUICK LOOK UNIT

FUNCTIONAL DESCRIPTION

The quick look unit provides two 16-bit binary registers with Amperex indicator triodes to display in binary form telemetry data words: frame sync, subcom sync, and experimenter's data, and eight 8-bit digital-to-analog converters to record data on a strip chart in analog form. The outputs from the D/A converters are fed to the oscillograph amplifiers which drive the CEC recording oscillograph. For flexibility in programming, eight auxiliary gates are included in the quick look unit.

The content of the main shift register, the words/frame counter, the three frames/subcom counters, and EW are all available at the patch panel of the unit. Any of these data may be monitored by using the binary registers, or as many as eight groups of eight bits each may be converted to analog signals for recording by the oscillograph.

Patching of data into the decimal display unit is done at the quick look unit patch panel. Thus any of the data available at the patch panel may be displayed in decimal form by the decimal display unit.

THEORY OF OPERATION

Binary Registers

The two binary registers are identical. Figure III-25 is the logic diagram for register no. 1; figure III-26 is the logic diagram for register no. 2. Each register consists of 16 FA's connected for parallel information drop-in. Input data is fed to the set and reset level controls on each FA. All ac set and reset inputs are tied together to form a common strobe line. When this line goes positive the data at the level controls are dropped into the individual FA's. An FA will assume the set or reset state depending on which level control input is at the "zero" level when the strobe line is pulsed. That is, if a set level control is at "zero" when the register is strobed, then the FA will assume the set condition.

The indicators are driven by the set output of each FA, e.g., FA24, pin 28. Therefore, in order to display the true (one) data bits, the set and reset level controls of each FA must be patched respectively to the true and complementary outputs of the shift register or counter stages. Now, when the data lines are strobed the false outputs (positive) will enable the FA's to be reset, thus providing positive levels to drive the indicators.

Strobing of data into the registers is accomplished by means of gating the EW pulse with any main or subcom frame word the data of which is to be displayed.

The patchable inputs to PA22 and DI23 are used to multiplex two additional data words so as to enable the display of three alternate words per frame by each register. The selection of words to be displayed is made by patching the corresponding word counts of the W/F or subcom counters and EW to the driver gate or any of the auxiliary gates. Patch panel pins and signals are given in figure III-27.

With the CONTINUOUS-SINGLE toggle switch in the CONTINUOUS position, the display changes as the input data changes. With the switch in the SINGLE position, depressing the push button switch will hold a particular display for as long as desired. The push button switch grounds one leg of the strobe line input NAND gate. With this gate inhibited the strobe line is inoperative and new data cannot be placed in the register. The data in the register at the time the push button switch is depressed remains there until the switch is released and a strobe pulse arrives.

Digital-to-Analong Converters

The eight digital-to-analog converters are all identical. Their logic diagrams are figures III-25 through III-28. Each converter consists of an eight-bit input register, and two LP-30 D/A converters connected to receive an eight-bit input. The reference potential for the LP-30's is -10 volts.

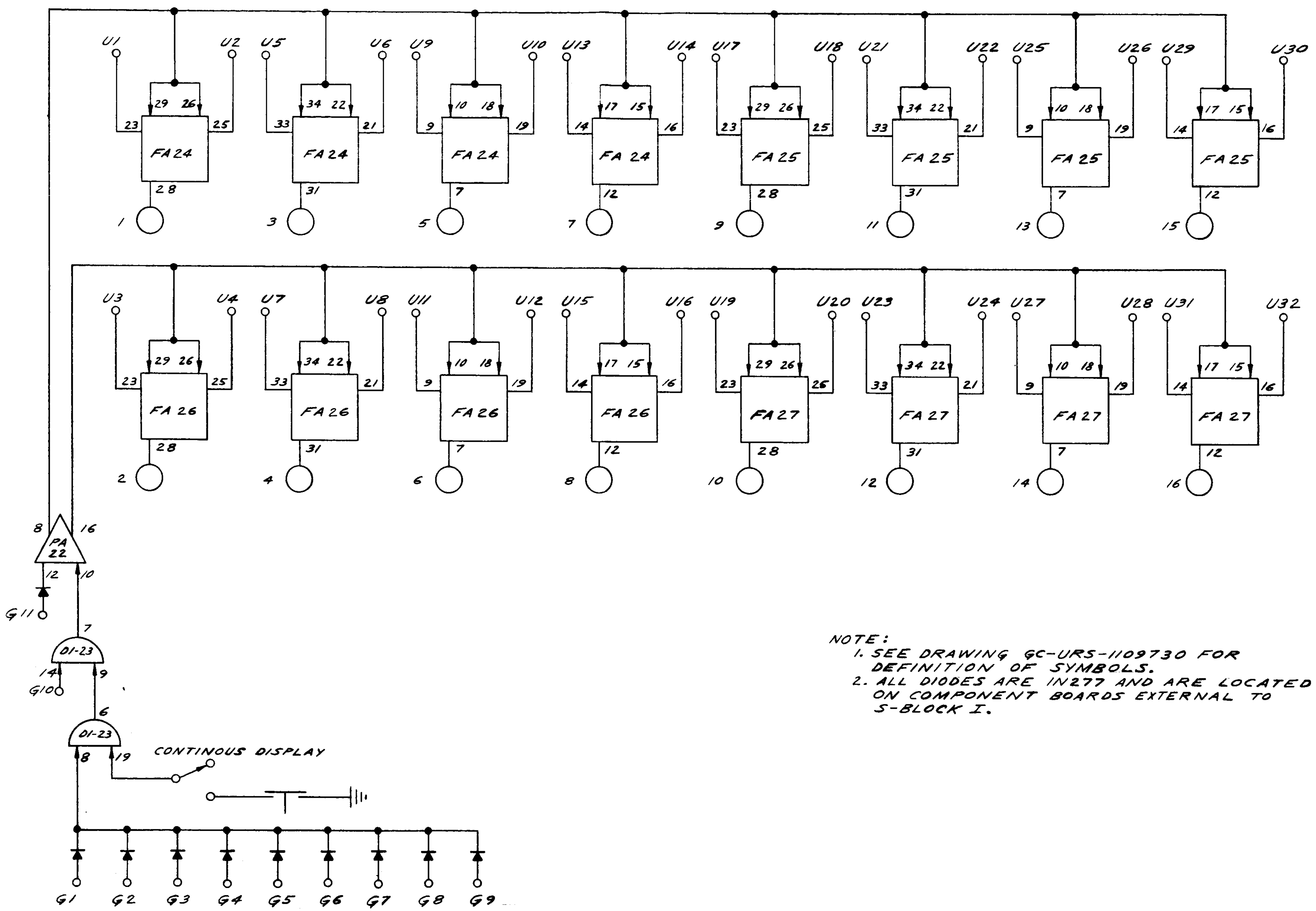
The input registers are connected for parallel information drop-in and function in the same manner as the two binary registers. The analog output voltage from the LP-30's is a portion of the reference voltage, and is determined by the combination of "ones" and "zeros" at the input. If the input is all "zeros" the full reference voltage will appear at the output. As the combinations of input bits increase in numerical value, the output voltage increases in the positive direction until an all "ones" input gives a 0-volt output.

The output from the D/A converters must be amplified to drive the recording oscillograph galvanometers. This is done in the oscillograph amplifier. The oscillograph amplifier is a GSFC-designed unit. It is discussed in Section V, Special Circuits, of this manual.

Auxiliary Gates

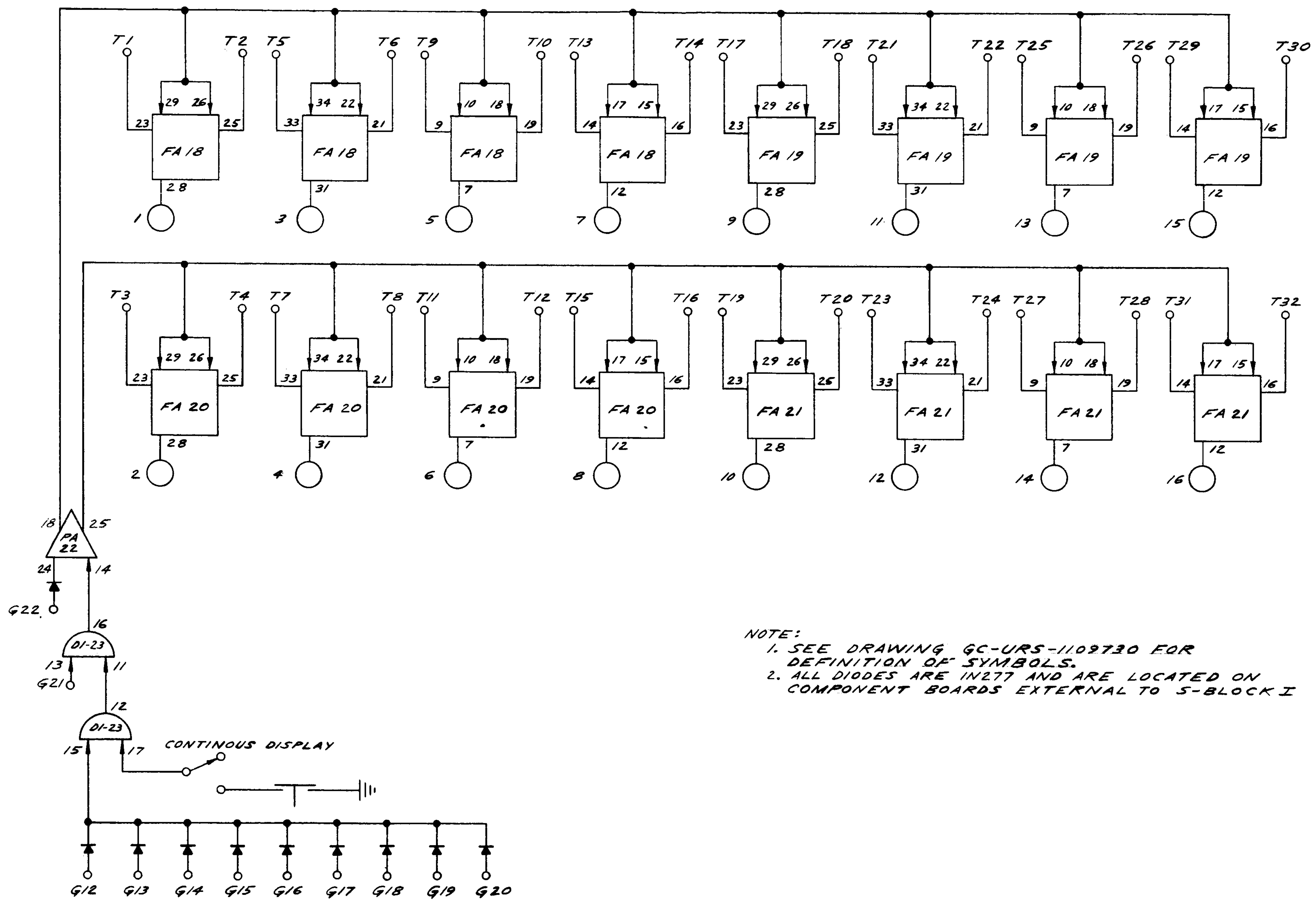
Eight auxiliary gates are included in the quick look unit (fig. III-27). They may be used, for example, to obtain strobe pulses by patching into the outputs of the counter stages available at the patch panel. Since patching for the decimal display unit is done at the quick look unit, the gated EW pulse needed by the decimal display is obtained by using auxiliary gate no. 7 and no. 8.

Each gate has eight input legs. A buffer-diode is connected in series with each input. The cathodes of all the input diodes for a gate are connected to the node of a DI. The outputs of gates no. 7 and no. 8 are fed to the decimal display unit through a rear connector. Gate no. 7 is used to supply the gated EW pulses for Word B of the decimal display, and gate no. 8 serves the same purpose for Word A.



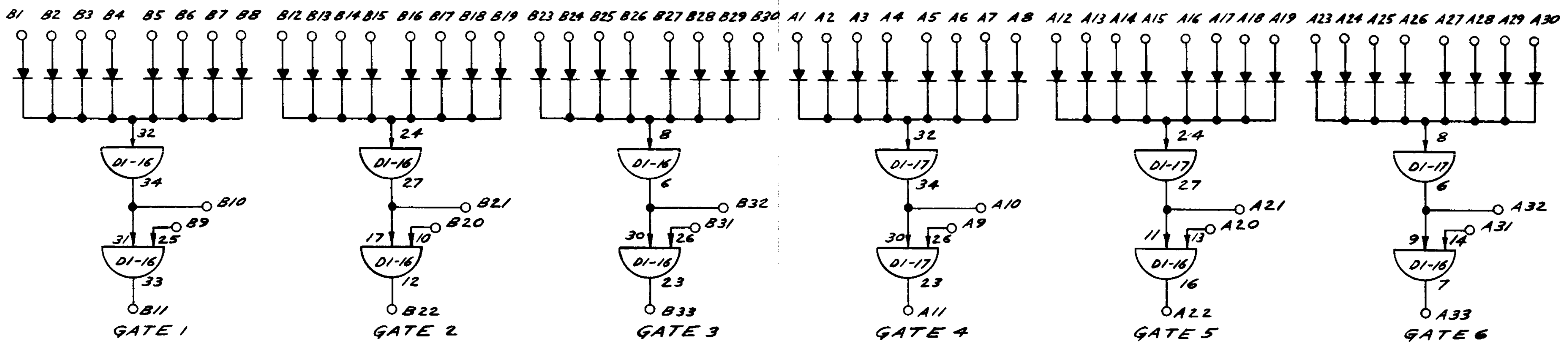
NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.
2. ALL DIODES ARE IN277 AND ARE LOCATED ON COMPONENT BOARDS EXTERNAL TO S-BLOCK I.

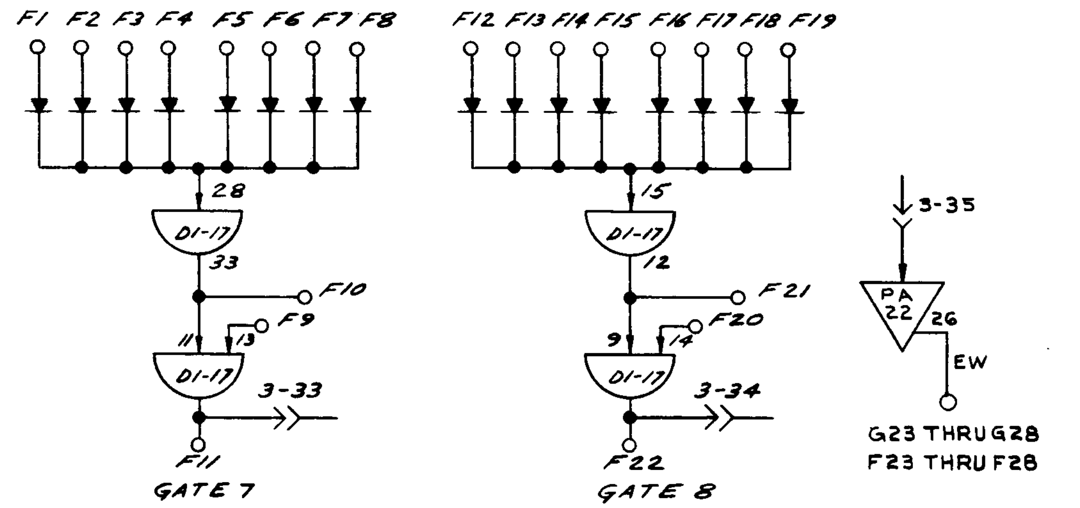
Figure III-25. Binary Register 1



NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.
2. ALL DIODES ARE IN277 AND ARE LOCATED ON COMPONENT BOARDS EXTERNAL TO S-BLOCK I

Figure III-26. Binary Register 2





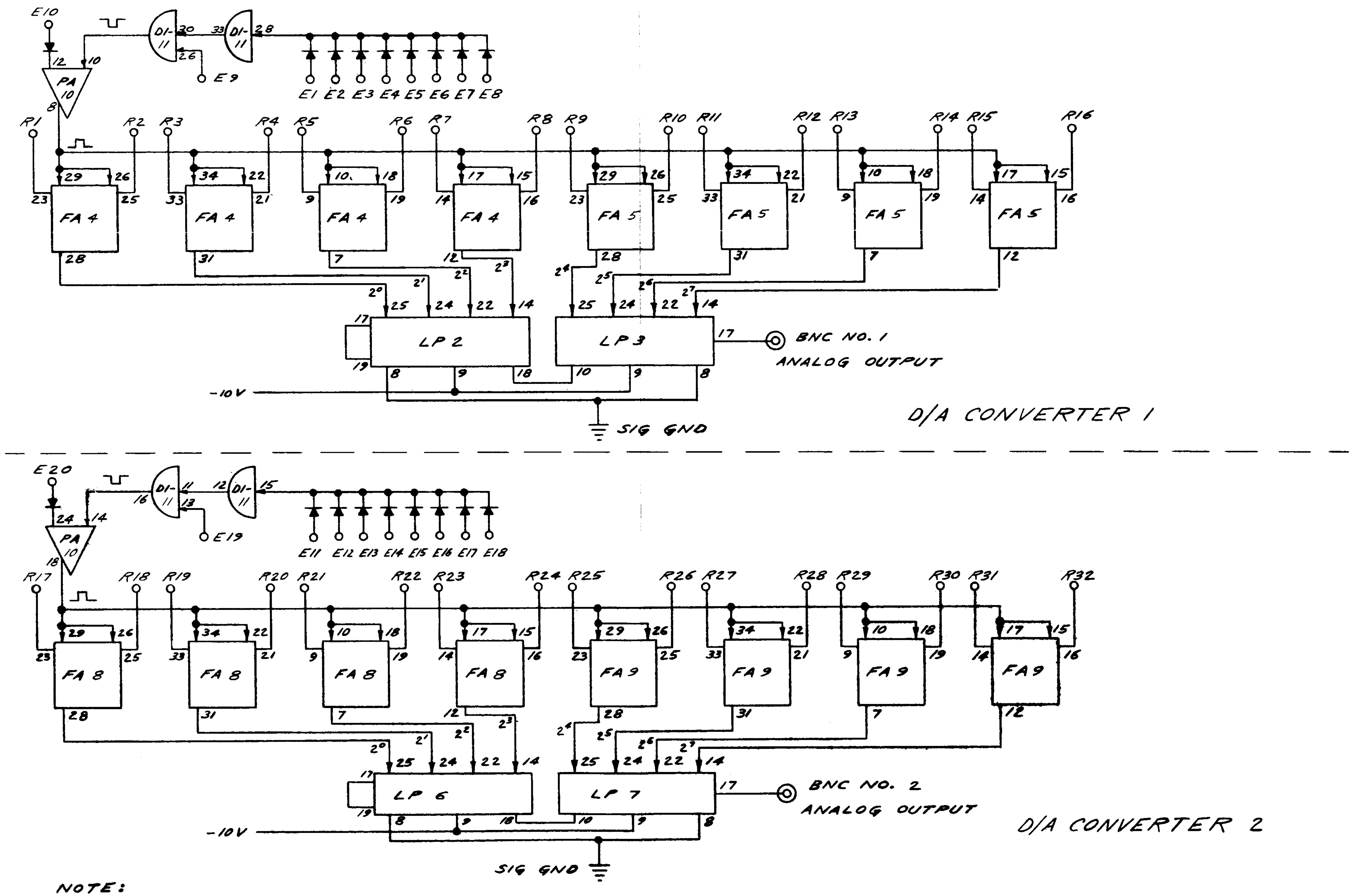
FROM CONNECTOR	TO PATCH PANEL	FUNCTION
Q-1-1	-Z1	$SR-2^0$
⋮	⋮	
Q-1-32	Z32	$SR-2^{31}$
Q-2-1	V1	$\overline{SR}-\overline{2^0}$
⋮	⋮	
Q-2-32	V32	$\overline{SR}-\overline{2^{31}}$
Q-3-1	S1	FOR DATA TO B/BCD CONVERTER SHIFT REGISTERS.
⋮	⋮	
Q-3-32	S32	
Q-4-1	J1	$W/F-2^0$
-2	J2	$-\overline{2^0}$
⋮	⋮	
-13	J13	2^6
-14	J14	$W/F-\overline{2^6}$
-15	J15	$SC1-2^0$
-16	J16	$-\overline{2^0}$
⋮	⋮	
-27	J27	-2^6
Q-4-28	J28	$SC1-\overline{2^6}$

PATCH PANEL
PINS C33 THRU Z33
AND A34 THRU Z34
ARE GROUND

CONNECTOR	PATCH PANEL	FUNCTION
Q-5-1	H1	$SC2-2^0$
-2	H2	$\overline{SC2-2^0}$
⋮	⋮	
-11	H11	$SC2-2^5$
-12	H12	$\overline{SC2-2^5}$
-13	H13	$SC3-2^0$
14	H14	$\overline{SC3-2^0}$
⋮	⋮	
-23	H23	$SC3-2^5$
Q-5-24	H24	$\overline{SC3-2^5}$

NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.

Figure III-27. Auxiliary Gates



NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.
2. ALL DIODES ARE IN277 AND ARE LOCATED ON COMPONENT BOARDS EXTERNAL TO S-BLOCK I

Figure III-28. Digital-to-Analog Converter 1 and 2

G. DECIMAL DISPLAY

FUNCTIONAL DESCRIPTION

The decimal display unit converts an input binary number to BCD, and provides a Nixie display of its decimal equivalent. It contains two identical binary-to-BCD converters with Nixie displays, each of which will accept an input of up to 16 bits. Each converter consists of a control circuit and five decade converters. Since the largest decimal number which can be represented by 16 binary bits is 65, 535, the five decade converters and five Nixie tubes are required for each binary-to-BCD converter.

Input data for the decimal display unit is obtained from the patch panel of the quick look unit (fig. III-27), thus any of the data available there may be fed into the decimal display. Except for sharing a common patch panel the decimal display and quick look units operate completely independently of each other.

THEORY OF OPERATION

General

Each binary-to-BCD converter consists of a control circuit, five decade converters, and five Nixie drivers. The display labeled WORD A on the front panel of the unit is identified in the figures as Binary/BCD Converter No. 2; WORD B is identified as Binary/BCD Converter No. 1. Logic diagrams for converter no. 1 are figures III-29 and III-30 (typical); for converter no. 2, figures III-31 and III-32 (typical). In the discussion which follows reference is made to figure III-29, the control circuit for binary-to-BCD converter no. 1, and to figure III-30, decade no. 1 of the same converter. The Nixie drivers are discussed in Section V, Special Circuits.

Control Circuit

The control circuit (fig. III-29) generates the necessary shift and strobe pulses (except for the initial strobe pulse) to perform the binary-to-BCD conversion. It also contains a 16-stage shift register to receive the binary input from the quick look unit patch panel. The last stage of the shift register serves as the least significant bit stage for decade converter no. 1 (fig. III-30). For this reason, only 15 shift pulses are required for each conversion cycle. Following the 15th shift pulse the bit in the first stage of the shift register (the 2^0 stage) will be in the last stage (the 2^{15} stage) where it represents the least significant bit for the least significant digit of the Nixie display. The last stage of the shift register is therefore the only stage which may ever require resetting.

A conversion cycle is started by the arrival of a gated EW pulse. This pulse has four functions:

1. It resets the decade register stages (BC's) in the five converter decades.

2. It strobes the shift register input gates, setting a "one" into each stage of the shift register which has a "one" at its input gate. (Loads the binary data word to be converted.)

3. It resets the last stage of the shift register if the stage is in the "one" state from the previous conversion cycle, and the input to the stage for this cycle is a "zero".

4. It enables outputs from the MV which are used to generate the shift and strobe pulses for every conversion cycle.

As shown in Figure III-29, two distinct signals are generated by the converter control circuits: Reset and Strobe pulses. The reset pulse is derived from the GEW pulse which is stretched from 2 us to 10 us. This duration is necessary in order to reset all 20 stages of the 5 converter decades. The trailing edge of this pulse is used to set FA2-28 which enables the MV pulses. These pulses are used to generate the strobe pulses which shift the contents in the shift register and complement the decade stages.

To begin with, the strobe pulse counter is reset by $\overline{\text{ER}}$ so that DN6-9 has a positive level. This inhibits the PA from sending out the first MV3-6 pulse. The first pulse is counted, however, and thus DN6-9 becomes negative to enable the next and subsequent pulses to be passed by the PA. These pulses are illustrated in figure III-33. It is seen that only 15 pulses are passed for every conversion cycle. The 16th pulse fills the counter which resets FA2-28 and causes DN6-9 to go positive again. This action disables the MV pulses and prevents the first MV pulse of the next conversion cycle from passing through the PA. The generation of 15 strobe pulses is now completed. The next cycle is started with the arrival of the next gated end-of-word (GEW) pulse. The second part of the conversion process takes place in the converter decade circuits as described in the following paragraphs.

Binary-To-BCD Conversion

Figure III-30 is the logic diagram for decade no. 1 of binary-to-BCD converter no. 1. It functions as the least significant digit decade of this converter. Reference will be made to figure III-30 in the following discussion as typical of all decades. It functions like the other four decades, except that its least significant bit decade register stage is the last stage (2^{15}) of the shift register.

The binary-to-BCD conversion process consists of 15 unique operations for the 16 bit word, one operation per bit. Each operation takes place throughout the entire 5 decade converter. However, actual logic functions are performed beginning in decade no. 1 and progressed through the remaining decades as the word bits are shifted in the shift register one by one.

The conversion of a pure binary number of 16 bits into its BCD equivalent is accomplished by (a) establishing a 5 decade register, (b) examining the contents of each register and adding "3" to that whose contents are 5 or greater, and (c) shifting the contents of each register by one bit from the least to the most significant bit and decade.

Table III-1, line 6 shows the strobe pulses used to effect conversion in each decade. The first bit is already in decade no. 1 by virtue of its being in the 2^{15} stage of the S.R. which is the least significant stage of this decade. The leading transition of the 2nd strobe pulse shifts the 2nd bit in the S.R. The positive strobe pulse causes the proper decade register stage(s) to be complemented by the corresponding DN, thus shifting the contents by one bit. The new contents in the decade register are now examined (decoded) by the OD during the negative strobe pulse. When the next positive strobe pulse occurs the proper decade register stages are complemented again, etc. This is repeated 15 times until all bits have been shifted through the shift register, decoded by the OD's in groups of four, passed through the decade registers, and finally placed in the proper register stages so that by the end of the 15th strobe pulse the OD's are ready to decode the contents of each decade register and drive their decimal indicators.

Table III-1 presents the actual conversion steps performed in each decade to convert binary 22214 into decimal 22214. The underlined bit (most significant) indicates its propagation through the converter decade stages as it was being shifted in the conversion process. It is seen that addition of "3", wherever required, and shifting is accomplished simultaneously, but independently of the shifting in the S.R. In fact, the leading transition of the strobe pulse shifts the S.R. contents for the following operation.

The 2^{15}th stage of the S.R. is not actually complemented in this process. It is shown as such only to carry through the complete BCD equivalent in this decade as it is done in the other ones. It should be noted that stages in each bracket form the 4 stage decade registers for each BCD digit of the 16 bit binary number.

Table III-2 shows the operation performed on each stage of a decade register for a particular output decoded from its OD. The D, C, and B stages are either complemented or left unchanged. The A stage is reset if the OD output is from decimal 0 to 4, and set if the output is from decimal 5 to 9. The prime on the A stage indicates that it belongs to the previous decade.

Each decade converter consists of an OD-30 connected in the BCD-to-decimal configuration, a NOR gate matrix, and a four-stage decade register. The stages of the decoder registers are designated B, C, D, and A, with the "B" stage representing the most significant bit, and the "A" stage representing the

Table III-1. Binary-To-Decimal Conversion

Shift Register (S.R.) Stages — Converter Decades

Pulse	2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}	2^0 2^{15}	① D 2^1	C 2^2	B 2^3	A 2^0	② D	C	B 2^3	A 2^0	③ D	C	B 2^3	A 2^0	④ D	C	B 2^3	A 2^0	⑤ D	C	B 2^3 *	A
GEW	0	1	1	0	0	0	1	1	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
S1		0	1	1	0	0	0	1	1	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
S2			0	1	1	0	0	0	1	1	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
S3				0	1	1	0	0	0	1	1	0	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
																	0*	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
S4					0	1	1	0	0	0	1	1	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
S5						0	1	1	0	0	0	1	1	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
S6							0	1	1	0	0	0	1	1	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
S7								0	1	1	0	0	0	1	1	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	
																	1*	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	
S8									0	1	1	0	0	0	1	1	1	1	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	
																	1	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	
S9										0	1	1	0	0	0	1	1	1	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	
																	0*	1	0	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	
S10											0	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	
																	0	0	1	0	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	
S11												0	1	1	0	0	0	0	0	1	0	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	
																	1*	1	0	1	1	1	0	1	1	1	0	0	1	0	0	0	0	0	0	0	
S12													0	1	1	0	0	1	1	0	1	1	1	0	1	1	1	0	0	1	0	0	0	0	0	0	
																	1*	0	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	
S13														0	1	1	1	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	
																	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	
S14															0	1	1	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	
																	0*	1	0	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	
S15																0	0	0	1	0	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	
																		4				1				2				2				2			

Converted decimal equivalent 22214

GEW - Loaded binary equivalent of 22214 into S.R.

S - Strobe pulse, leading transition, shifted one bit in S.R., and the pulse proper operated on the decade circuits to add "3" and shift.

* - For clarity only, actually does not change states.

OD Output	D	C	B	A
0	-	-	-	R
1	C	-	-	R
2	C	C	-	R
3	-	C	-	R
4	-	C	C	R
5	-	C	-	S
6	-	C	-	S
7	C	-	-	S
8	C	C	C	S
9	-	-	-	S

NOTE: C = Complement

R = Reset

S = Set

- = No Change

Table III-2. Decade Register Complementing for Decoded OD Outputs least significant bit of the next higher decade. The "A" stage for the decade no. 1 is actually the last stage (2^{15}) of the shift register. Since the last shift register stage also functions as a decade register stage, the last decade register stage of decade no. 5 is not needed and serves no purpose in the conversion process.

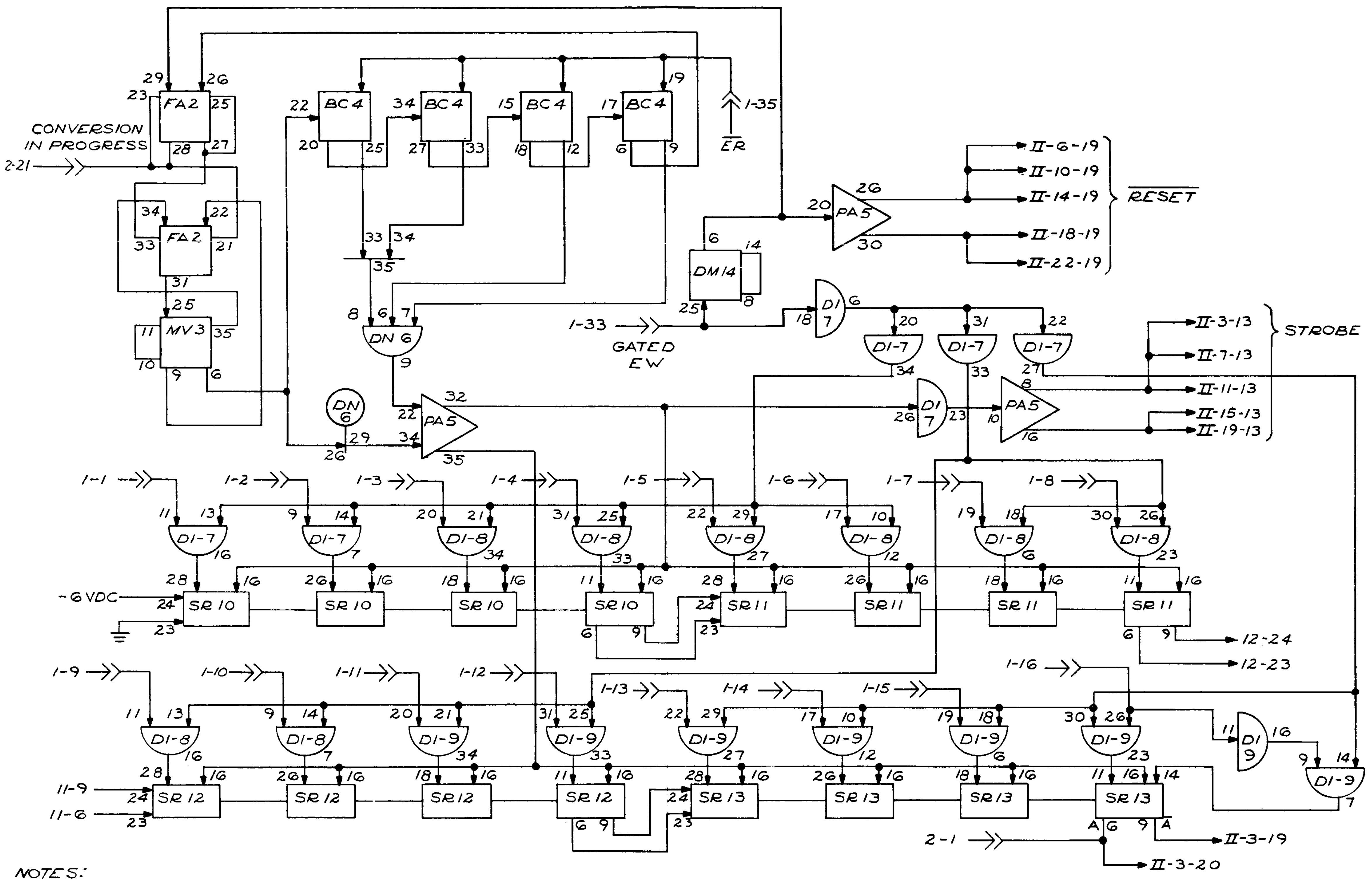
Data is shifted from the shift register into pins 19 and 20 of OD3 in decade converter no. 1. The decoded output of the OD is fed through the NOR matrix into the decade register. The outputs of decade register stages B, C, and D are fed back to the input of OD3. Register stage A's output is fed to the input of OD7 in decade converter no. 2. This same arrangement is also used in decade converters no. 3, 4, and 5.

Figure III-34a illustrates two examples of shifting operations in a decade register. Figure III-34 is a simple shift operation when the decoded OD output is two; figure III-34b illustrates the addition of three to the decade register and shifting for a decoded OD output of five. Note in this case that the addition of three to the decade register automatically shifts the contents.

Referring to figure III-34a and figure III-30, decade no. 1 of binary-to-BCD converter no. 1, assume that following a shift pulse the decade register contains a BCD two. The OD decodes this input and pin 8 of the OD (the decimal two output pin) goes positive. As a regult, NOR gate outputs DN4-9, DN4-13, and DN5-13 go negative. When the next strobe pulse arrives the outputs of these gates will undergo a positive transition. This complements decade register stages D and C, and resets Stage A. Stage B is unchanged. According to Table III-1, these are the required operations when a BCD two is decoded. Figure III-34 shows that it has been shifted one place to the right.

For a BCD five input a count of three must be added in the shifting operation, so the decade register must contain a BCD eight when the operation is completed. When the OD decodes the BCD five input, pin 34 of the OD goes positive and NOR gate outputs DN4-13 and DN5-9 go negative. When the strobe pulse arrives decade register stage C is complemented and stage A is set. Stages D and B undergo no change. Figure III-34b shows that the decade register now contains a BCD eight.

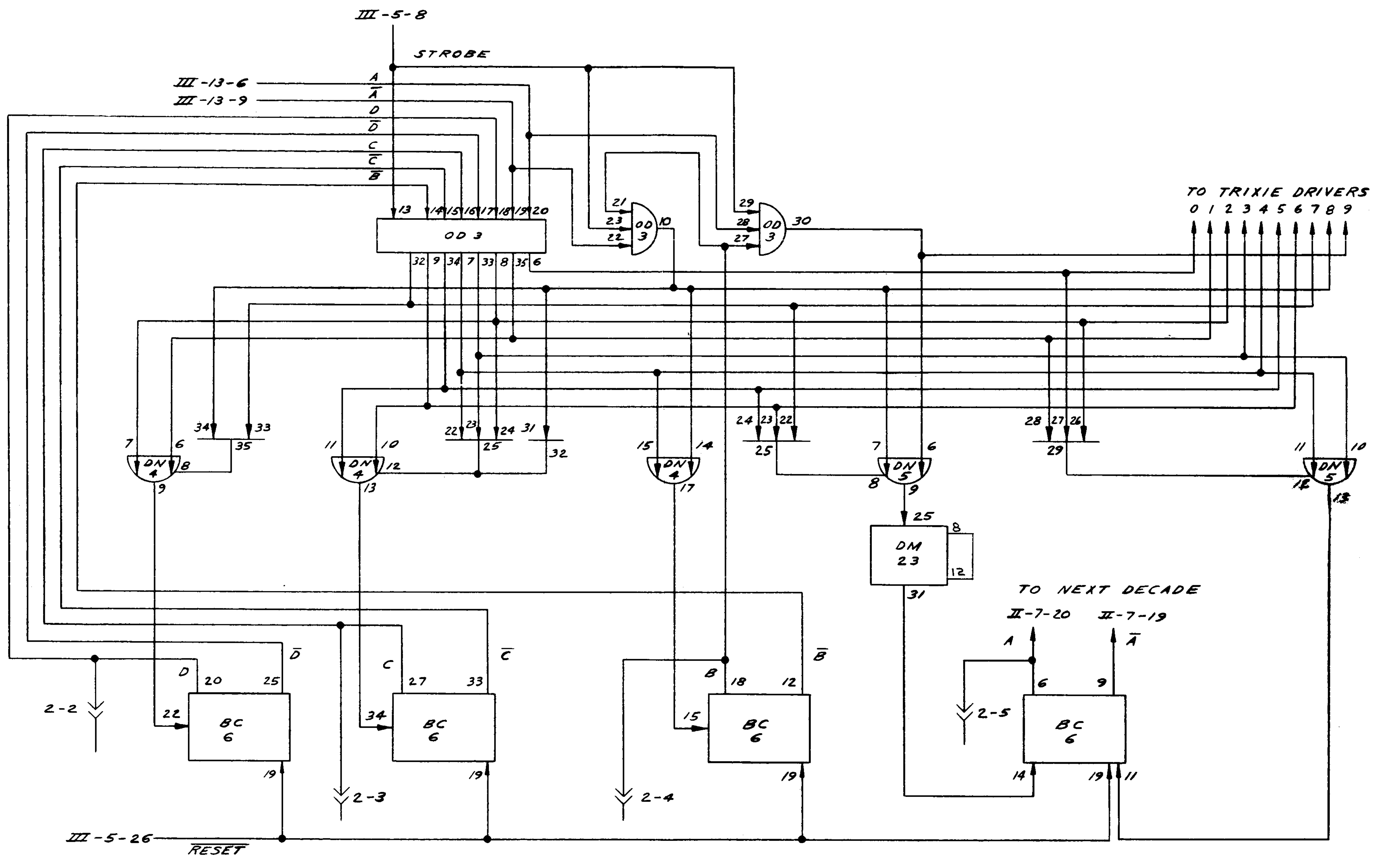
Following 15 shift-strobe pulses the binary-to-BCD conversion is completed. The decoded output from the five OD's at this time is the decimal equivalent of the binary input to the unit. This is displayed until a gated EW pulse is received to start a new conversion cycle.



NOTES:

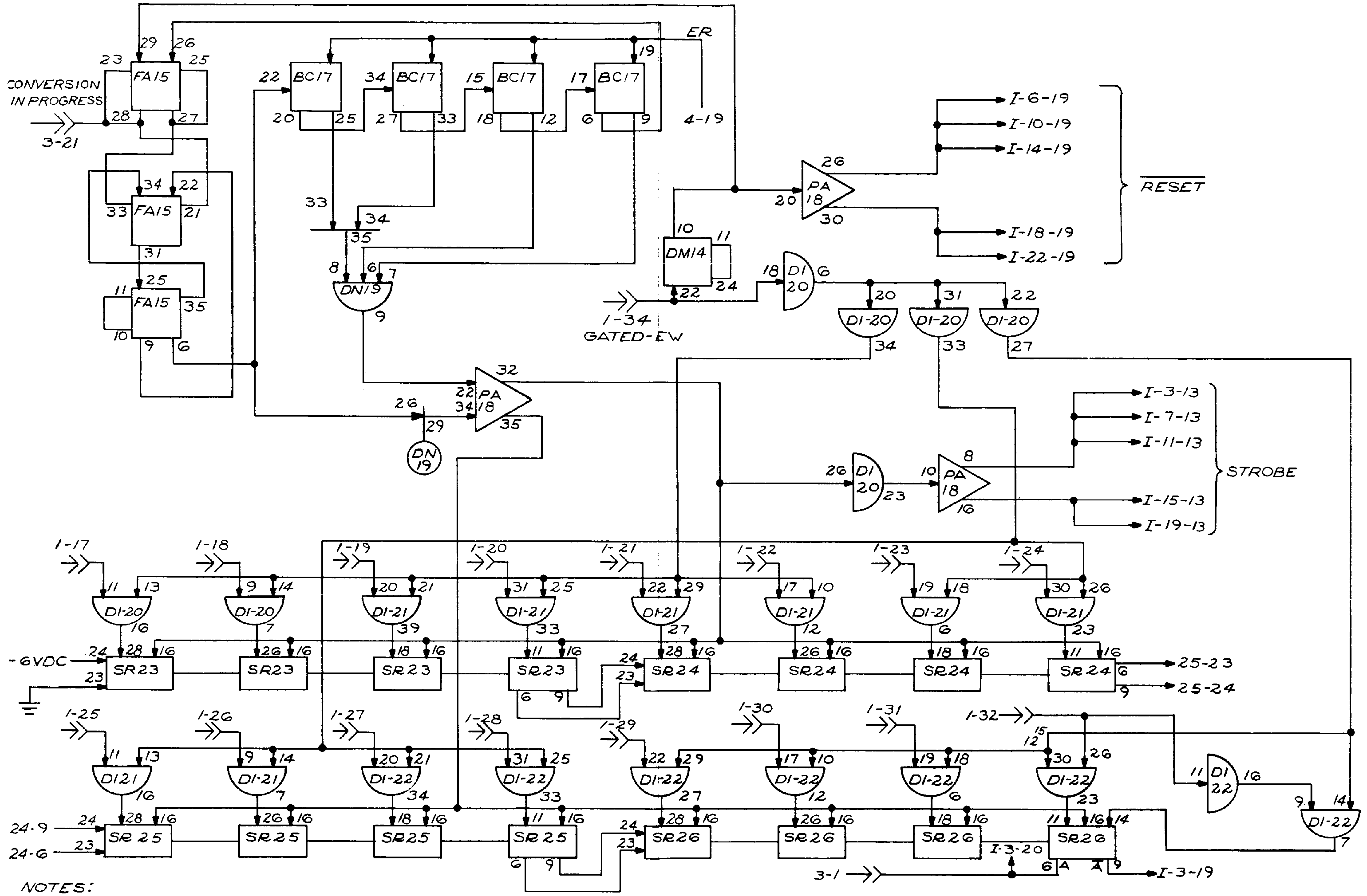
1. (a) CONNECTOR PINS 1-1 THRU 1-16 ARE WIRED TO QUICK LOOK UNIT PATCH PANEL PINS S1 THRU S16 RESPECTIVELLY.
   (b) APPLICABLE INPUTS ARE PATCHED TO "TRUE" LOGIC SIGNALS, AND REMAING INPUTS ARE GROUNDED, SEE DRAWING GC-URS-1109804.
2. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.

Figure III-29. Binary/BCD Converter Control 1



NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.

Figure III-30. Binary/BCD Converter 1, Decade 1 (typical)

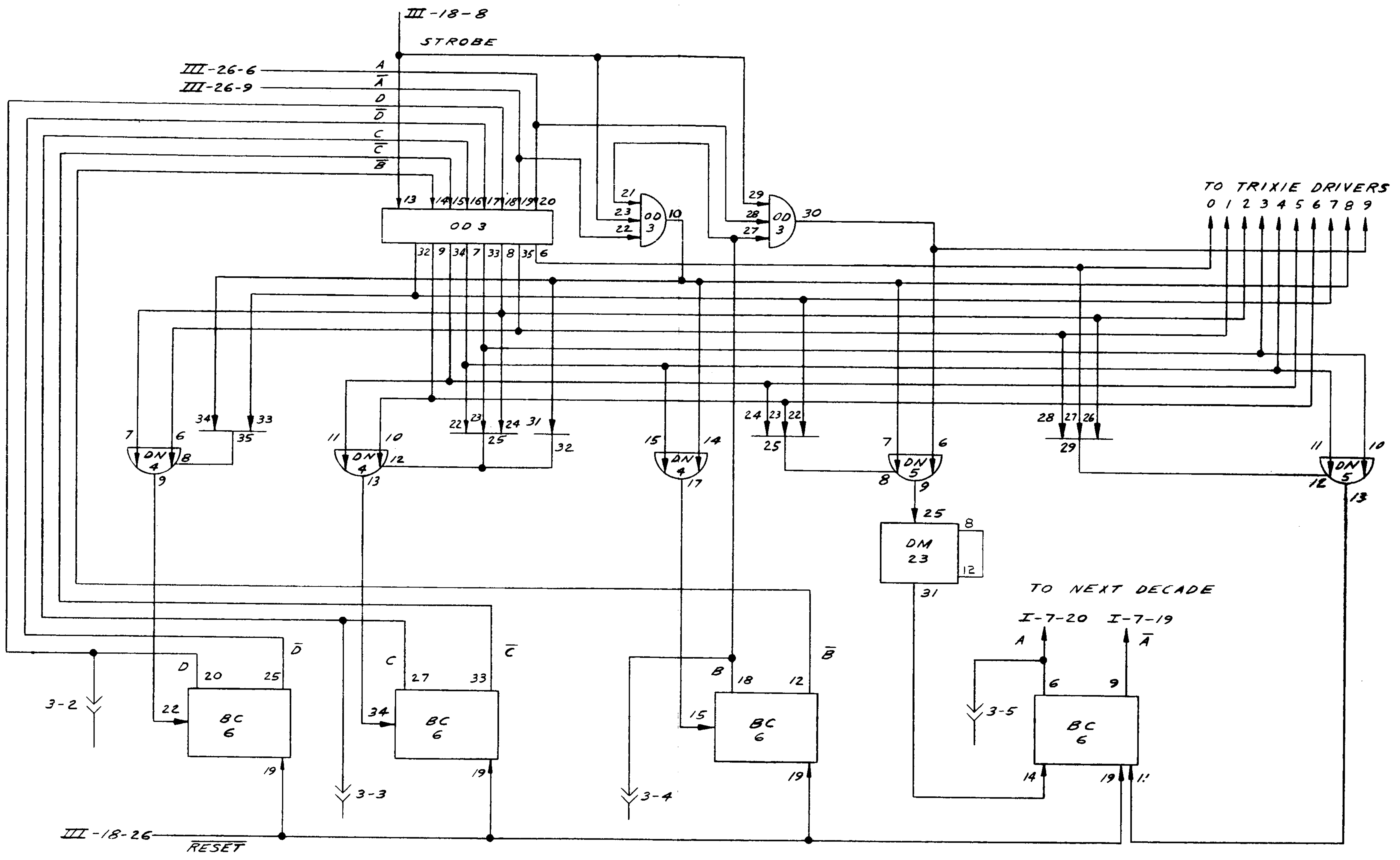


NOTES:

1. (a) CONNECTOR PINS 1-17 THRU 1-32 ARE WIRED TO QUICK LOOK UNIT PATCH PANEL PINS S17 THRU S32 RESPECTIVELY.
   (b) APPLICABLE INPUTS ARE PATCHED TO "TRUE" LOGIC SIGNALS, AND REMAINING INPUTS ARE GROUNDED, (SEE DWG. GC-URS-1109804).

2. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.

Figure III-31. Binary/BCD Converter Control 2



NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.

Figure III-32. Binary/BCD Converter 2, Decade 1 (typical)

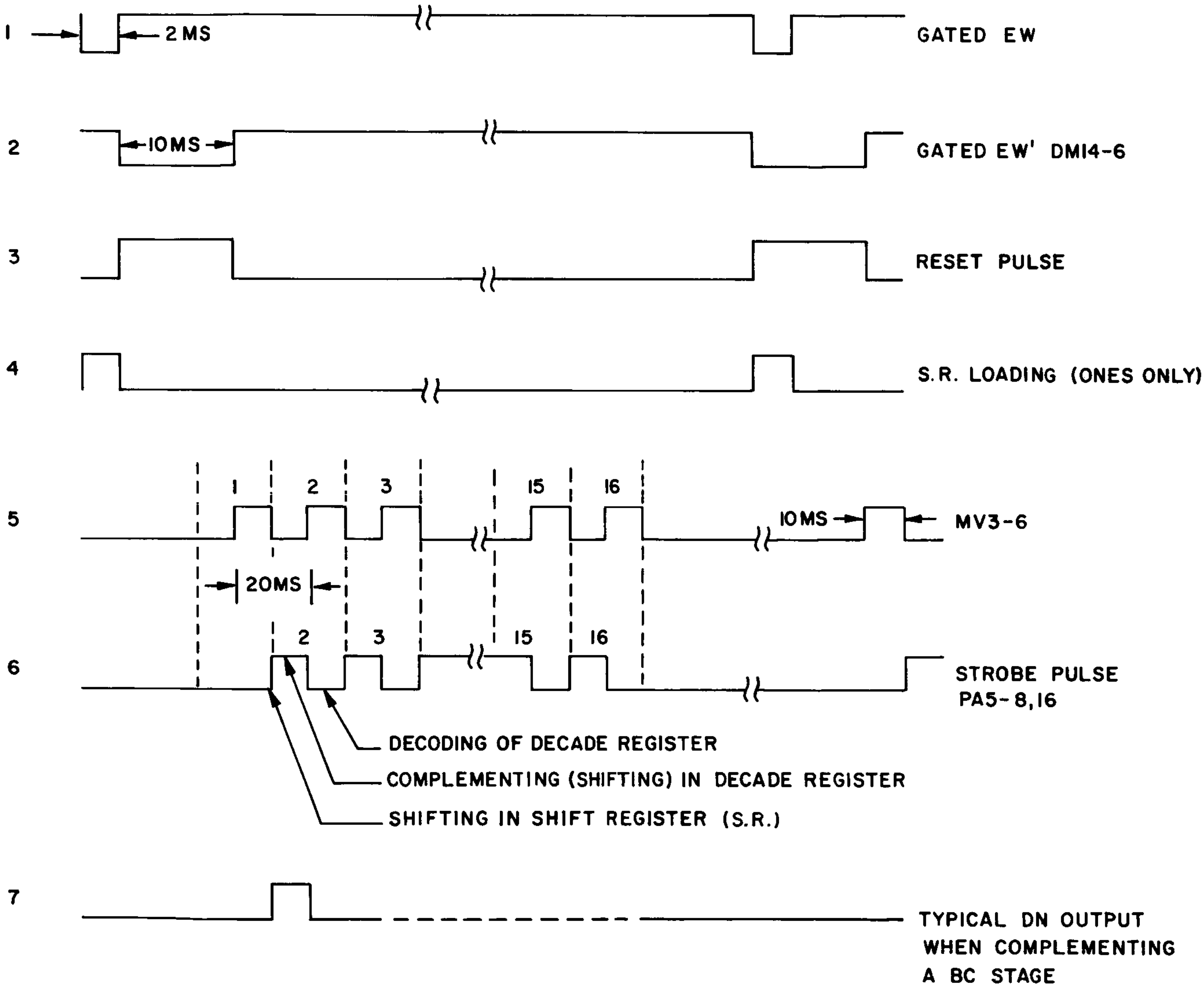


Figure III-33. Reset and Strobe Pulses

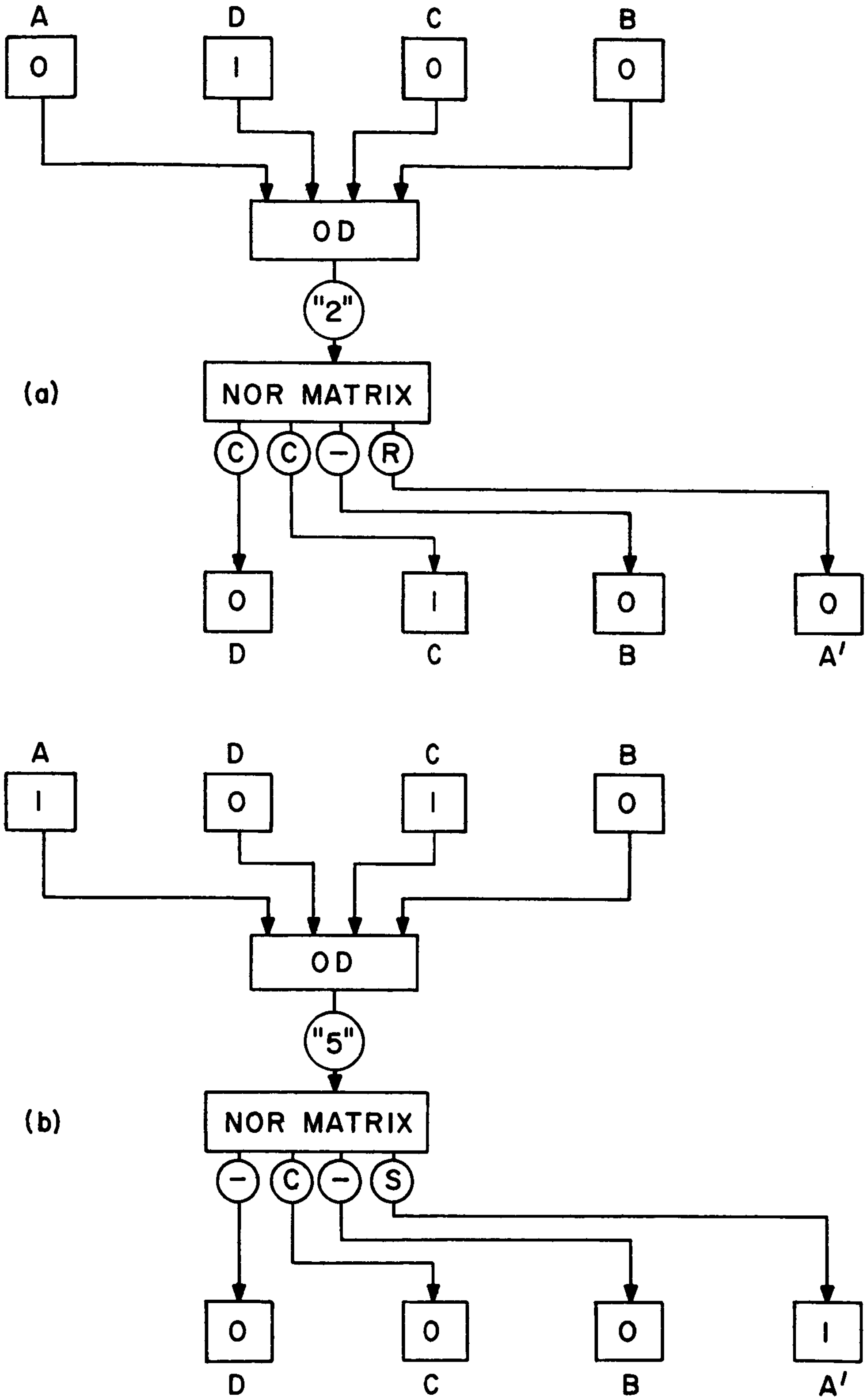


Figure III-34. Examples of Decade Register Data Shifting

General Notes:

1. All logic circuits, except Error Detectors, and those designated by "*" used in this system are made by Computer Control Company, Inc. (3C).

2. Reference should be made to "Instruction Manual For S-Pac Digital Modules", dated 11 April 1962, for detail description and schematic diagram of all 3C logic circuits.
URS-1110100

3. Refer to System Interconnection Wiring List, Dwg. No. for interconnection of System Units.

Definitions of Symbols

A. Logic Circuits

Note: The "30" series of 3C circuits is used throughout.

BC - Binary Counter
DI - NAND Gate
DM - One Shot (Delay Multivibrator fixed width)
DN - NAND Gate and auxiliary diode gates
FA - Flip-Flop
LP - Digital-to-Analog Converter (D/A)
MV - Multivibrator Clock (astable multi)
OD - Octal Decimal Decoder
PA - Power Amplifier
SR - Shift Register
ST - Schmitt Trigger
UI - Unit Indicator
DMA - One shot (variable width)

B. Signals

Notes: 1. Logical "One", or true logic signal, corresponds to -6v, and logical "Zero" corresponds to 0v.

2. A positive signal is defined as a change from -6v to 0v, and is designated by a bar (-) over the symbol.

3. A negative signal is defined as a change from 0V to -6v, and is designated by the symbol proper.

4. Unless defined otherwise, symbols in juxtaposition describe one signal in terms of their respective definitions, e.g., WL - Word Lock, etc.

S - Sync
L - Lock
WS - Word Sync (in phase)
WS' - Word Sync (out-of-phase)
FS - Frame Sync (in-phase)
FS' - Frame Sync (out-of-phase)
W - Word
F - Frame
ER - External Reset
FR - Frame Reset
WR - Word Reset
Øi - In phase
Øo - Out-of-phase
EW - End of word pulse
EF - End of frame pulse
B/W - Bits per word
W/F - Words per frame
SC - Subcom
DL - Data Delete
CTR - Counter
Adv - Advance
E - Error
D/A, A/D - Digital-to-Analog, Analog-to-Digital
P - Parity (Po, Pe - odd, even)
Aux - Auxiliary
Ex - Excessive
TP - Time present
DP - Data present
FL - Flag
B/BCD - Binary-to-Binary Coded Decimal
FIL - Filter
G - Gated
FSW' - False Frame Sync Word Pulse (Bad)
EW' - False End of Word Pulse (Bad)

C. Circuits, Signal Flow, and Interconnection

—Indicator Triode, No. 6977

UI — Unit Indicator, 3C

—Logic Circuit: Amplifier

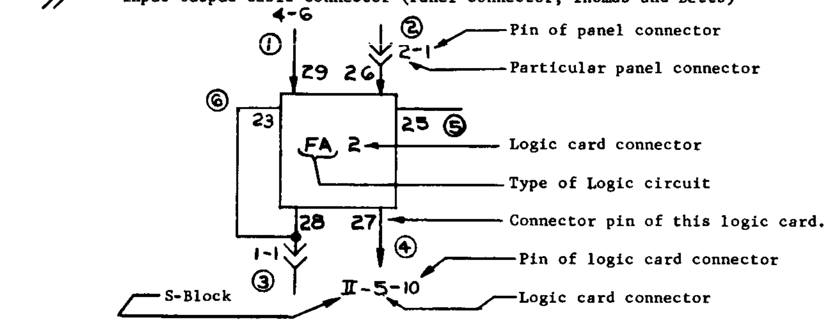
—Logic Circuit: FA, BC, SR, DM, MV, etc.

— Signal Input (Pulse or Level)

—Logic Circuit: DI, DN

— Patch Panel Pin

— Input-Output Cable Connector (Panel connector, Thomas and Betts)



Note: The following explanation of the meaning and usage of the above symbols applies to all logic circuits contained in this System, unless otherwise specified.

1 Signal Input from logic card connector No. 4, pin 6 of the same S-Block as indicated in the drawing title block. A positive going signal (pulse) produces a negative output at 3. Likewise, a positive signal at 2 produces a negative output at 4. The input-output lines are collinear. The sense of direction of the panel connector symbol at 2 and 3 indicates, respectively, the incoming and outgoing signal. 5 and 6 are gate inputs for signals 2 and 1 respectively. These inputs must be positive in order to pass the signals and produce the outputs.

Interconnection of S-Blocks (there are 3 S-Blocks in every unit) is indicated by Roman numerals preceding the connector-pin numbers.

Figure III-35. Definition of Symbols

Table IV-1

B. Programming of the Search and Lock Unit

Function (Performed by one or more circuits)	Associated Patch Panel Pins	
	Input Pin(s)	Signal Source Pin(s)
Data input	C15	A1 for split-phase A2 for modified split phase
Clock input	C17	D16 direct D17 divided by 2
Word Sync Recognition:		
In-phase	B1, B3, B5	V2, V4, V6 - True
Out-of-phase	B2, B4, B6	V1, V3, V5 - False
Frame Sync Recognition:*		
In-phase	S1, S3, S5. . . S15	V1, V2, V3. . . V15, V16
	N1, N3, N5. . . N15	R1, R2, R3. . . R15, R16
	J1, J3, J5. . . J15	M1, M2, M3. . . M15, M16
	E1, E3, E5. . . E15	H1, H2, H3. . . H15, H16
Bit Error Compensation	D1, D2, D3, D4, D5, D6	C6
Out-of-phase	S2, S4, S6. . . S16	U1, U2, U3. . . U15, U16
	N2, N4, N6. . . N16	Q1, Q2, Q3. . . Q15, Q16
	J2, J4, J6. . . J16	L1, L2, L3. . . L15, L16
	E2, E4, E6. . . E16	G1, G2, G3. . . G15, G16
Bit Error Compensation	D7, D8, D9, D10, D11, D12	C7
Frame Synchronization:		T18, T20, T22, T24, True Search Counter Outputs
In-phase, Enter Search Status	R17, R19, R21, R23	T17, T19, T21, T23, False Search Counter Outputs
Flywheeling	R18, R20, R22, R24	
In phase, Enter Lock Status	U18, U20, U22, U24	V18, V20, V22, V24-True Lock Counter Outputs V17, V19, V21, V23-False Lock Counter Outputs
	C18	D18, for frame sync only
	C23	D23, for word and frame sync only
Out-of-phase, Enter Search Status	K18, K20, K22, K24	L18, L20, L22, L24-True outputs L17, L19, L21, L23-False outputs
	P19	Q19, for frame sync.
	P21	Q21, for frame sync.
		C12 or C13, for word and frame sync only.

SECTION IV

PROGRAMMING

A. INTRODUCTION

Because of the different telemetry data formats employed, the Data Processor must be programmed for each specific format associated with a particular spacecraft. The programming is of "hard ware" type, requiring selection of certain circuits, input-output configurations, and buffer command timing. This kind of programming is accomplished by means of selective patch panel wiring. There are five patch panel assemblies whose panels are to be wired by means of multiple pin jumpers and inserted into the panel frames.

Wiring Tables

The following five tables, IV-1 to IV-5, describe the functions to be selected and patch panel pins to be interconnected to accomplish these functions. Each table is given for the unit in which the patch panel is located. When wiring these panels, reference should be made to the figures describing the unit, to make sure that the proper connections are secured. Complete wiring information for two satellite formats OSO (S-17) and OGO (S-49) is given at the end of this section, which should serve as an example and guideline for other PCM telemetry data formats.

Interpretation and Use of Tables

The programming tables contain three columns of information: (a) Function, (b) Input Pins, and (c) Signal Source Pins. The "function" column indicates the functions performed by one or more circuits in the unit. The "input" column gives the circuit patch panel pins to which input signals (pulses or levels) must be applied to generate the function. The "signal source" column shows the patch panel pins which provide the required signals. It should be noted that not all pins are always interconnected to generate the indicated functions. For example, in Table IV-1, for the "in phase frame lock counter" function, the pins to be interconnected are determined by the number of "good" frames required to ascertain "frame lock", e.g., in case of 3 frames, pins U18 and U20 are connected to V18 and V20, the other pins are left unused. Therefore, knowledge of the required format and theory of operation of this equipment is essential to properly interconnect the patch panel pins.

In "Signal Source" column, counter output pins from left to right represent binary counts in increasing order, i.e., 2^0, 2^1, 2^2, etc. Likewise, main shift register outputs are given in increasing order of binary weighting.

Notes and footnotes should be consulted to determine which of the many indicated signal sources are applicable to a particular buffer tape format.

Table IV-1

B. Programming of the Search and Lock Unit (Cont'd)

Function (Performed by one or more circuits)	Associated Patch Panel Pins	
	Input Pin(s)	Signal Source Pin(s)
Out-of-phase,		Q20, for word and frame sync only.
Enter Lock Status	M18, M20, M22, M24	N18, N20, N22, N24-True outputs N17, N19, N21, N23-False outputs
	P17	Q17, for frame sync. Q18, for word and frame sync only.
Frame or Word Reset Signal	P23	Q23, for frame sync Q24, for word and frame sync only.
Word Synchronization:**	B10	C9 or C11 (depending on sync bits)
In-phase, Enter	B8	C8 or C10 (depending on sync bits)
Search Status	E17, E19, E21, E23	G18, G20, G22, G24-True outputs
Flywheeling	E18, E20, E22, E24	G17, G19, G21, G23-False outputs
In phase, Enter Lock Status	H18, H20, H22, H24	J18, J20, J22, J24-True outputs J17, J19, J21, J23-False outputs
	C19	D18, for frame and word sync only.
Word Reset Signal	C20**	D19, for frame sync D20, for frame and word sync only.
Word Search Light	C21**	D21, for frame sync only

Table IV-1

B. Programming of the Search and Lock Unit (Cont'd)

* All inputs not patched to the Shift Register must be patched to GROUND. (See figure III-3)

"True" outputs are designated by <u>even</u> numbered pins and "false" outputs are designated by <u>odd</u> numbered pins. U1, V1 and U2, V2 represent the least significant $(2^0, 2^0)$ stage; and H15, G15 and H16, G16 represent the most significant $(2^{31}, 2^{31})$ stage. For less than 32 bits per word, the shift register outputs are truncated from right to left, e.g., for a 16 bit word the first 16 stages from left to right are used and the last 16 stages are truncated.

** Except for C20 and C21, inputs for this function shall be patched only when "word sync" is used together with "frame sync". C20 and C21 shall be patched to the appropriate sources in either case as indicated.

Table IV-2

C. Programming of the Accumulator Unit

Function (Performed by one or more circuits)	Associated Patch Panel Pins	
	Input Pin(s)	Signal Source Pin(s)
Buffer Commands:*		
Data Present	A7, See Note 2	J17 special case (S-17) G14 normal (S-49)
	K15	K16, See note 1
Time Present	J2	E16
		K18, K20...K24 True W/F
	F1, F2... F6	J19, J21.. J23 counter output
		K19, K21...K23 False W/F
	See note 3	J18, J20.. J24 counter outputs
	F7	B1
Alternate Data Present	F8, F9... F13	See note 3
	F14	B1
Subcom Sync	G7	B3
Dump	A8	B2
Frame Sync Confidence	A10	A12
	A11	B20
Frame Sync Flag	C15	C18
	D11	A12 or proper frame word
Bit Counting	G15	C2, 2^0 stage of S. R. to count "1" bits
	G16	C18
	H13	H12
	H14, H15	A16, Resets Counter
Word Counting	G15	E18
	J10, J11, G8, G9, G10, G11, G12	H8, H9, H10, H12, H3.. H6, True outputs
		H7, H11, False counter outputs
Divide by "2"	H1, H2	G13
	A22	A13, Resets once/ frame

Table IV-2

C. Programming of the Accumulator Unit (Cont'd)

Function (Performed by one or more circuits)	Associated Patch Panel Pins	
	Input Pin(s)	Signal Source Pin(s)
Subcom Sync Pulse Generation	J8	E8 or A12 See note 4
	J7	F7 or E8 See note 4
	J6	J5
	J4	J3 or J9 See note 4
Buffer Register Loading and Generation of Data Present Pulse	H17	A13
	K17	K18 See note 5
	D1	E18 See note 5
Multiplexing	K6	G14 See note 6
Buffer Output Data	K5	A13 See note 6
Buzzer	K14	K13
Expanding the Data Register	K11, K12, J15, J16, A20	B10, A1, A2, B16, B2**
	K9, K10, B23	From Auxiliary Flag Flip-Flops
Miscellaneous***	D12, D16, C8, C12, B7, B9, B14	See note 7
	E1, E2. . . E7,	
	E9, E10. . . E13	
	A3	
	A4, A23	
	J14	
	K1	

* All commands are not always required. Whichever command is not required, one of its gate inputs must be patched to GROUND.

** These connections should be used to expand the buffer data register only. Otherwise, the inputs are to be used whenever special data, or flag bits, e. g., S-17, have to be sent to the buffer.

*** Circuits (gates, flip-flops, one-shots) are provided for the purpose of generating special functions which might be required by various buffer tape formats. Inputs to these circuits are given to identify each available circuit. The signal sources are not listed because they may vary with each format. A thorough knowledge of the format requirements and circuit operation is necessary in order to make proper use of and connections to these circuits.

Table IV-2

C. Programming of the Accumulator Unit (Cont'd)

NOTES:

1. This is the normal connection as is done in S-17. For S-49, the signal is derived from 2 sources and added through Gate 4. Therefore, K15 is connected to A6 in place of K16.

2. Normally, data present command pulses are generated periodically at the end of every word or multiple words. In case of 3 or more words G14 provides the proper signal. In S-17, the commands are generated every 2 words, and are obtained from K18 (2^0 stage of the W/F counter).

3. Time present commands may be derived from the W/F counter if they are to be given within the frame, or from the EF pulse if they are required at the end of each frame (S-49). Likewise, the alternate data present commands may be derived from the same sources (Word 30 for S-17).

4. Whenever telemetry data is subcommutated and the computer format requires data block synchronization with respect to a subcom channel (word), a subcom sync pulse is generated which produces the buffer command. Depending on the subcom sync word location and requirement for subcom sync flagging, the signal can be generated at the end of word following detection or end of frame. In S-17, for example, it is generated at the end of word 30, thus J8 is connected to E8. In S-49, it is generated at the end of frame, therefore, J8 is connected to A12. Similarly, for S-17, J7 is connected to F7, and for S-49, J7 is connected to E8. The inputs to the gate of E8 are obtained from the appropriate W/F or subcom counter stages. Also, in S-17, the subcom sync command is given to the buffer every other time, therefore, J4 is connected to J3, whereas for S-49, it is connected to J9.

5. These connections are valid only for data present pulses to be generated every 2 words, e.g., (S-17). In other cases, e.g., S-49, additional "loose" circuits must be used to provide the proper input signals.

6. Multiplexing is enabled by triggering K5 and disabled by triggering K6. To permanently disable it connect K6 to A13, e.g., S-17, where it is not used.

7. Outputs of the word/frame and all subcom (frames/subcom) counters are given in Figure III-19.

Table IV-3

D. Programming of the B/W/F Counters Unit

Function (Performed by one or more circuits)	Associated Patch Panel Pins	
	Input Pin(s)	Signal Source Pin(s)
Generation of End of Word Signals (EW)	Y1, Y2, Y3, Y4, Y5	Z1, Z3, Z5, Z7, Z9 - True outputs Z2, Z4, Z6, Z8, Z10 - False outputs
	Y10	S16
	Y9	U16 for frame sync only T16 for word and frame sync only
Generation of Frame Sync Word (FSW) Signals and End of Frame Pulse	W8, W9, W10, W11, W12 W13, W14	X1, X3, X5, X7, X9 X11, X13 - True outputs X2, X4, X6, X8, X10, X12 X14 - False counter outputs
FSW, $\overline{\text{FSW}}$, and FSW'	V1, V3, V5, V7, V9, V11, V13 V2, V4, V6, V8, V10, V12, V14*	U1, U2, U3, U4, U5, U6, U7*
	U13	U16
	U14	S16
EF	W1, W2, W3, W4, W5, W6, W7	X1, X3...X13 - True X2, X4....X14 - False
Subcom Synchronization** (Normal)		
Frames/Subcom No. 1	P14	Q16 or U1 (inverted)
	R1, R2, R3, R4, R5, R6, R7, R8	T1, T3, T5, T7, T9, T11, T13 - True outputs T2, T4, T6, T8, T10, T12, T14 - False outputs
	S1, S2, S3, S4, S5, S6, S7, S8	X1, X3, X5, X7, X9, X11, X13 - True output X2, X4, X6, X8, X10, X12, X14 - False output
Subcom Counter No. 1	Q1, Q3, Q5, Q7, Q9, Q11, Q13	D21, D22, D23, D24, D25, D26, D27

Table IV-3

D. Programming of the B/W/F Counters Unit (Cont'd)

Function (Performed by one or more circuits)	Associated Patch Panel Pins	
	Input Pin(s)	Signal Source Pin(s)
Correction	Q2, Q4, Q6, Q8, Q10, Q12, Q14	D28, D29, D30, D31, D32, D33, D34
	F21, F22, F23, F24, F25, F26, F27, F28, F29, F30, F31, F32, F33, F34	Fourteen outputs, 7 true and 7 false, are obtained from the S. R. See fig. III-9
	E21, E22, E23. . E34	T1, T2, T3, T4, T5, T6. . T13, T14
	C34	S14
Correction Flywheel	C31, C32, C33	C25, C27, C29 - True counter outputs C26, C28, C30 - False outputs
Multiple Subcoms***	Q1, Q3, Q5, Q7, Q9, Q11, Q13	P1, P2, P3, P4, P5, P6, P7
	Q2, Q4, Q6, Q8, Q10, Q12, Q14	Only when presetting to "0"
	S9, S10, S11, S12, R9, R10, R11	T1, T3. . . T13 - True outputs T2, T4. . . T14 - False outputs
	P14	N16
	S13	P18
	P16	M18
	G16	R14
Subcom Sync	N19, N20. . . N34	Z19, Z20. . Z34-True outputs
Recognition No. 1	P19, P20. . . 34	V19, V20. . . V34 - True outputs U19, U20. . . U34, Q19, Q20. . . Q34 False shift register outputs, see fig. III-9
Bit Error Compensation	H20, H21, H22, H23, H24, H25	H26

Table IV-3

D. Programming of the B/W/F Counters Unit (Cont'd)

Function (Performed by one or more circuits)	Associated Patch Panel Pins	
	Input Pin(s)	Signal Source Pin(s)
Subcom Sync Recognition No. 2	M19, M20... M34 L19, L20... L34	Same as for no. 1
Bit Error Compensation	G20, G21, G22, G23, G24 G25	H28
Subcom Sync Recognition No. 3	K19, K20...K34 J19, J20... J34	Same as for no. 1
Bit Error Compensation	H29, H30, H31, H32, H33, H34	G26
Subcom No. 1	Q1, Q3... Q13	P1, P2, P3, P4... P7 presets counter.
Synchronization	Q2, Q4... Q14	P1, P2... P7 presets counter to "0" only
(See figure III-16)	R1, R2, R3, R4... R8	T1, T3... T13 True counter outputs. See Note 3. T2, T4... T14 False counter outputs
	S9, S10, S11, S12, R9, R10, R11	T1, T2... T14, counter outputs, see note 1.
	S1, S2, S3... S8	See Note 2
	P16	L18, (S-17, special case)
	G16	R14 (S-17, special case)
	P14	N16 (S-17, special case)
Subcom No. 2	K1, K2...K12	J1, J2.. J6 Presets counter
Synchronization (See figure III-15)	L1, L2... L8	See Note 2
	M9, M10... M14, L9	See Note 1
	M1, M2... M8	N1, N3... N11, True counter outputs. See Note 3. N2, N4... N12, False counter outputs
	J14	L16 (S-17, special case)
	L10	P18 (S-17, special case)
	M16	L18 (S-17, special case)
	H16	L14 (S-17, special case)

Table IV-3

D. Programming of the B/W/F Counters Unit (Cont'd)

Function (Performed by one or more circuits)	Associated Patch Panel Pins	
	Input Pin(s)	Signal Source Pin(s)
Subcom No. 3 Recognition	E1, E2. . . . E12	D1, D2. . . D6, presets counter
(See Fig. III-14)	F1, F2. . . F8	See Note 2
	G9, G10. . . G14, F9, E16	See Note 1
	G1, G2. . . . G8	H1, H3. . . H11, True outputs. See Note 3. H2, H4. . . H12, False outputs
	D14	J16
	F10	P18
	K16	L18
	F16	F14

See Note 4.

* When the counter is to be preset to "0" use these inputs in place of V1, V3. . . . V13.

** This function is for synchronous subcommutation only, e.g., OGO (S-49), having one subcom which is updated and corrected by the spacecraft's subcom counter. For asynchronous subcoms, like S-17, this patching does not apply.

*** Asynchronous subcommutation as in the OSO (S-17) satellite, where two independent subcoms are used, requires special programming and is considered herein as a special case. Therefore, a thorough knowledge of the format, and operation of the three Frames/Subcom Counters is required (See Section III, B/W/F Counters Unit) whenever similar formats are to be programmed. This part of patching does not apply to synchronous subcommutation as in S-49.

Table IV-3

D. Programming of the B/W/F Counters Unit (Cont'd)

NOTES:

1. This gate is used to decode subcom word(s) wherein the subcom sync code or verification code is to be found, e.g., S-17. It may also be used for other functions requiring the decoding of certain counts and "clocking" them in conjunction with signals associated with the subcom synchronization process.

2. This gate is used to preset the subcom counter to a particular count or zero. In the S-17 case, this is preset to "0" when the following signals are in coincidence: Word 2 or 18 of the main frame and recognition of subcom sync (S13 receiving a negative pulse from P18). Similar preset gates are used for subcom 2 and 3 counters to preset them when subcom sync is recognized in coincidence with the corresponding main frame word(s). In fact all three frames/subcom counters perform identical functions in synchronizing three independent subcoms.

3. The reset gate is used to reset the counter at a particular count, i.e., all "true" outputs are set to "0" when a given count is decoded. For example, in S-17, the counter is reset at the count of "48".

4. It should be noted that there are three subcom sync recognizers (fig. III-11 through III-13), intended for use with each frames/subcom counter whenever each subcom has a unique sync code. However, when the same sync code is used for several subcoms, but located in different main frame words, as in the S-17 case, then the same recognizer may be used to detect the presence of this sync code, and applied to the preset gates of all counters involved.

Table IV-4

E. Programming of the Error Monitor Unit

Function (Performed by one or more circuits)	Associated Patch Panel Pins	
	Input Pin(s)	Signal Source Pin(s)
Parity Error Count and Indication	J22	H22 for even parity H21 for odd parity
	J21	K1
Frame Sync Error	E1, E2, E3.... E16	K1, K2, K3... K16 True S. R. Outputs
Count and Indication (See figure III-22)	D1, D2, D3... D16	J1, J2, J3.... J16 H1, H2, H3... H16 False S. R. Outputs G1, G2, G3.... G16
See Note		

NOTE:

The input pins are of the frame sync shift register. The source pins are of the main data shift register where the frame sync code is found. For proper operation, the input pins must be patched to the complementary frame sync code bits in the main shift register. For example, if the frame sync code is 10011000, then the first eight inputs must be patched to H1, K2, K3, H4, H5, K6, K7, K8, and all other inputs to Ground.

Table IV-5

F. Programming of the Quick Look Unit

Function (Performed by one or more circuits)	Associated Patch Panel Pins	
	Input Pin(s)	Signal Source Pin(s)
Binary Display of	U1, U3, U5.... U31	Z1, Z2, Z3... Z16 - True S. R. outputs 2^0 - 2^{15}
Data Words*	U2, U4, U6.... U32	V1, V2, V3... V16 - False S. R. outputs 2^0 - 2^{15}
(Register No. 1)	G1, G2.... G9	W/F Counter outputs or Subcom Counter outputs
	G10, G11	Gates 1 thru 6**
D/A Conversion	R2, R4.... R16	Z1, Z2, Z3.... Z8
of Data Words	R1, R3..... R15	V1, V2, V3.... V8
For Strip Chart	E1, E2, E3.... E8	W/F Counter Outputs and EW
Recording *** (Converter No. 1)	E10, E9	***

* There are two identical 16 bit binary displays which can be programmed to display two 16-bit words or one 32-bit word by patching proper shift register outputs(figure III-27), to the appropriate binary register stages. Listed herein are connections of the first 16 bits (2^0 - 2^{15}) to be displayed for one of the registers. The second is patched similarly.

** If more than one word per frame is to be displayed auxiliary decoding gates 1 thru 6 can be used to load the data of the desired words. The EW signals, G23-G28, must be patched to every gate used.

*** There are eight 8-bit digital-to-analog converters to convert and record eight channels of digital data. Each channel may contain one or more words. If several words are to be converted per channel, auxiliary gates 1 thru 6 should be used to supply strobing pulses. The EW pulse must be applied to every gate used. The other converters are patched similarly to that listed herein.

Table IV-5

G. Programming for the Decimal Display Unit

Function (Performed by one or more circuits)	Associated Patch Panel Pins	
	Input Pin(s)	Signal Source Pin(s)
Binary-to-BCD	F12, F13.... F19	W/F Counter Outputs, and EW
Conversion, Word A	S17, S18.....S32	Z1, Z2... Z32 *
B/BCD Conversion,	F1, F2..... F18	W/F Counter Outputs, and EW
Word B	S1, S2.....S16	Z1, Z2.... Z32 *

* Conversion of binary data to BCD is limited to 16 bits per word. Proper bits (S. R. outputs) must be selected and patched to the inputs in order to convert and decimally display the desired data words. Inputs in excess of those used per word must be patched to Ground. (See figure III-19)

Patch Panel Wiring List For S-17

Search and Lock Patch Panel Wiring For S-17

Circuit and Function	Patch Panel Pins: From	Patch Panel Pins: To	Signals (Level or Pulse)			
Data Input	A1	C15				
Clock Input	C17	D17	Divide by 2 for NRZ			
In-phase frame sync recognizer	S1	V2	2^0		0	
	S3	V3	$\overline{2^1}$		1	
	S5	V6	2^2		0	
	S7	V8	2^3	Shift	0	
	S9	V9	$\overline{2^4}$	Register	1	
	S11	V11	$\overline{2^5}$	Outputs	1	
	S13	V14	2^6	(Comple-	0	True
	S15	V15	$\overline{2^7}$	ments	1	frame
	N1	R2	2^8	of	0	sync
	N3	R3	$\overline{2^9}$	the	1	code
	N5	R5	$\overline{2^{10}}$	frame	1	(Barker)
	N7	R7	$\overline{2^{11}}$	sync	1	
	N9	R9	$\overline{2^{12}}$	code)	1	
	N11	R12	2^{13}		0	
	N13	R14	2^{14}		0	
	N15	R16	2^{15}		0	
	J1 & E1	K1	GROUND			
	J3 & E3	K3	"			
	.	.	"			
	.	.	"			
	.	.	"			
	J15 & E15	K15	"			
	D2	C6	-6 vdc for 1 bit error			
Out-of-phase frame sync recognizer	S2	V1	$\overline{2^0}$		1	
	S4	V4	2^1		0	
	S6	V5	$\overline{2^2}$		1	
	S8	V7	$\overline{2^3}$	Shift	1	
	S10	V10	2^4	Register	0	
	S12	V12	2^5	Outputs	0	
	S14	V13	$\overline{2^6}$	(Comple-	1	False
	S16	V16	2^7	ments	0	frame
	N2	R1	$\overline{2^8}$	of	1	sync
	N4	R4	2^9	frame	0	code
	N6	R6	2^{10}	sync)	0	
	N8	R8	2^{11}		0	
	N10	R10	2^{12}		0	
	N12	R11	$\overline{2^{13}}$		1	
	N14	R13	$\overline{2^{14}}$		1	
	N16	R15	$\overline{2^{15}}$		1	

Search and Lock Patch Panel Wiring For S-17

Circuit and Function	Patch Panel Pins		Signals (Level or Pulse)
	From	To	
Out-of-phase frame sync recognizer (Cont'd).	J2 & E2	K2	GROUND
	J4 & E4	K4	"
	.	.	"
	.	.	"
	.	.	"
	J16 & E16	K16	"
	D8	C7	-6 vdc for 1 bit error
Word sync	D19	C20	Disables word reset ($\overline{WR}$)
(not used	D21	C21	Disables word lock & search lights
Frame Synchronization (In-phase)	V17	U18	2^0 Lock Counter
	V19	U20	2^1 Outputs.
	V22	U22	2^2 Locks after "5"
	V23	U24	2^3 valid frames.
	T18	R18	2^0 Search Counter.
	T20	R20	2^1 Flywheel 8 frames.
	T22	R22	2^2
	S17	R17	2^0 Search Counter.
	S19	R19	2^1 Begins searching
	S21	R21	2^2 immediately.
	S23	R23	2^3
			Search Pulse to effect
	C18	D18	"Lock" from out-of-phase.
	Q17	P17	FSW
	Q19	P19	FSW'
Frame synchronization (out-of-phase)	P21	Q21	FS'
	P23	Q23	Frame Search
	N17	M18	2^0 Lock Counter.
	N19	M20	2^1 Locks after "5"
	N22	M22	2^2 valid frames.
	N23	M24	2^3
	L17	K18	2^0 Search Counter.
	L19	K20	2^1 Begins searching
	L21	K22	2^2 immediately.
	L23	K24	2^4

B/W/F Counters Patch Panel Wiring For S-17

Circuit and Function	Patch Panel Pins From	Patch Panel Pins To	Signals (Level or Pulse)
B/W Counter, Establishing Words, 8 bits per word	Z1	Y2	2^0 B/W Counter Outputs "7" (8 bits)
	Z3	Y4	2^1
	Z5	Y5	2^2
	Y9	U16	$\overline{FR}$
	Y10	S16	$\overline{WFR}$
W/F Counter, Establishing Frames, 32 words per frame	W1 & W8	X1	2^0 W/F Counter Outputs "31" (32 bits) Establishes EF and resets W/F counter.
	W2 & W9	X3	2^1
	W3 & W10	X5	2^2
	W4 & W11	X7	2^3
	W5 & W12	X9	2^4
	U13	U16	$\overline{FR}$
	U14	S16	$\overline{WFR}$
	U1	V2	W/F Counter is preset to "0"
	U2	V4	
	U3	V6	
	U4	V8	
	U5	V10	
Subcom Sync Word Recog-nizer 1 to detect 0101.... (sync word)	P19	U19	$\overline{2^0}$ Shift Register Outputs for 01010101 sync code (MSB to LSB from left to right)
	P20	Z20	2^1
	P21	U21	$\overline{2^2}$
	P22	Z22	2^3
	P23	U23	$\overline{2^4}$
	P24	Z24	2^5
	P25	U25	$\overline{2^6}$
	P26	Z26	2^7
	H26	H20	-6 vdc for "0" bit errors
	P27 thru P34	P17	Ground
	N19 thru N34	N17	Ground
Subcom Sync Word Recog-nizer 2 to detect 1111.... (sync word verification)	M19	U19	$\overline{2^0}$ Shift Register Outputs for 11111111 sync code verification.
	M20	U20	$\overline{2^1}$
	M21	U21	$\overline{2^2}$
	M22	U22	$\overline{2^3}$
	M23	U23	$\overline{2^4}$
	M24	U24	$\overline{2^5}$
	M25	U25	$\overline{2^6}$
	M26	U26	$\overline{2^7}$
	H28	G20	-6 vdc for "0" bit errors
	M27 thru M34	M17	Ground
	L19 thru L34	L17	Ground

B/W/F Counters Unit Patch Panel Wiring For S-17

Circuit and Function	Patch Panel Pins From	Patch Panel Pins To	Signals (Level or Pulse)	
Frames/Subcom Counter 1, Wheel Subcom Synchronization Reset Gate	R1	T1	2^0	To reset counter at Subcom Word 48 and subcom sync. "47"
	R2	T3	2^1	
	R3	T5	2^2	
	R4	T7	$\overline{2^3}$	
	R5	T10	2^4	
	R6	T11	2^5	
	R8 & R11	S14	SC1S	
Auxiliary Gate	S9	T1	2^0	To detect & establish subcom sync word verification "15"
	S10	T3	2^1	
	S11	T5	2^2	
	S12	T7	$\overline{2^3}$	
	R9	T10	$\overline{2^4}$	
	R10	T12	$\overline{2^5}$	
	R14	G16	To strobe verification code	
Preset Gate	S1	X1	$\overline{2^0}$	W/F Counter Outputs, for Word 2 or 18, ("1" or "17") to preset subcom counter
	S2	X4	$\overline{2^1}$	
	S3	X6	$\overline{2^2}$	
	S4	X8	$\overline{2^3}$	
	S8	W16	EW	
	N16	P14	To advance subcom counter	
	S13	P18	Detected subcom sync word 0101....	
	P16	L18	Detected verification word 1111....	
Frames/Subcom Counter 1, Preset Gate	P1	Q2		From Preset Gate to preset the counter to "0"
	P2	Q4		
	P3	Q6		
	P4	Q8		
	P5	Q10		
	P6	Q12		
Frames/Subcom Counter 2, Sail Subcom Synchronization Reset Gate	M1	N1	2^0	To reset counter at Subcom word 48 and subcom sync. "47"
	M2	N3	2^1	
	M3	N5	2^2	
	M4	N7	$\overline{2^3}$	
	M5	N10	$\overline{2^4}$	
	M6	N11	2^5	
	M8 & L9	L11	SC2S	

B/W/F Counters Unit Patch Panel Wiring For S-17

Circuit and Function	Patch Panel Pins		Signals (Level or Pulse)	
	From	To		
Auxiliary Gate	M9	N1	2^0	To detect and establish subcom sync word verification
	M10	N3	2^1	
	M11	N5	2^2	
	M12	N7	2^3	
	M13	N10	$\overline{2^4}$	
	M14	N12	$\overline{2^5}$	"15"
	L14	H16	To strobe verification code	
Frames/Subcom Counter 2, Preset Gate	L1	X1	2^0	W/F counter outputs, for word 8 or 16, or 24 ("7" or "15" or "23") to preset subcom counter
	L2	X3	2^1	
	L3	X5	2^3	
	L4	F14	$\overline{W31}$	
	L8	W16	EW	
	L16	J14	To advance subcom counter	
	L10	P18	Detected subcom sync word 0101....	
	M16	L18	Detected verification word 1111....	
Preset Gate	J1	K2		From Preset Gate to preset the counter to "0"
	J2	K4		
	J3	K6		
	J4	K8		
	J5	K10		
	J6	K12		
Frames/Subcom Counter 3, Auxiliary Gate	G9	X7	2^3	W/F Counter outputs to inhibit W31 ($\overline{W31}$)
	G10	X9	2^4	
	K16	K17	GROUND	Maintain FA in Set state
	F16	Y16	C'	

Accumulator Patch Panel Wiring For S-17

Circuit and Function	Patch Panel Pins From	Patch Panel Pins To	Signals (Level or Pulse)
Data Present	K18	K17	2^0 W/F Counter
(DP)	E18	D1	EW
	J17	A7	$\overline{DP}$
	K16	K15	DP (delayed)
(WFL) (DL)	A13	H17	EF
	D18	G17	WFL
Time Present	K19	F1	$\overline{2^0}$
(TP)	K21	F2	$\overline{2^1}$ W/F Counter
	K23	F3	$\overline{2^2}$ Word 1
	J18	F4	$\overline{2^3}$
	J20	F5	$\overline{2^4}$
	E18	F6	EW
	B1	F7	(WFL) (DL)
	E16	J2	$\overline{TP}$
Alternate Data	K18	F8	2^0
Present (Flag 1)	K21	F9	$\overline{2^1}$ W/F Counter
	K22	F10	2^2 Word 30
	K24	F11	2^3
	J19	F12	2^4
	B1	F13	(WFL) (DL)
	E18	F14	EW
Subcom Sync	E1	H20	2^1
Gate 1:	E2	H22	2^2 Subcom Counter 1
	E3	H24	2^3 Word 47 or 48
	E4	G20	$\overline{2^4}$
	E5	G21	2^5
	E8	J8	
	J7	F17	$\overline{SC1S'}$
	J5	J6	
	J3	J4	
Flag 2:	G7	B3	Subcom Sync Pulse
Dump, Flag 3	A8	B2	Dump
Two Frames of	G15	C2	2^0 Shift Register
Ones: Counter	G16	C18	CD
	H14	H15	
	H14	E15	Counter Reset
	H12	H13	
	H3	J10	
	H4	J11	
	G11	A5	Word 30
Inverter 1	A3	F15	
Divide by 2	H1	H2	
	B20	G12	(FSQ) (2 F's of 1's)

Accumulator Patch Panel Wiring For S-17

Circuit and Function	Patch Panel Pins From	Patch Panel Pins To	Signals (Level or Pulse)
	A22	A13	EF
	J1	K9	Flag bit for 2F's of 1's
Playback Flag	K13	K14	
	B24	K10 & D4	Output to buffer and Indicator 19
Frame Sync	C15	F15	Word 30
Quality Flag	D11	A12	EF
	B21	D10	Indicator 22
Subcom 1 Flag	D14	F17	$\overline{SC1S'}$
	D12	G21	2^5, SC Counter 1
	D13	A12	EF
	D15	K11 & B23	Indicator 28
Subcom 2 Flag	D16	E23	2^5, SC Counter 2
	C6	D17	$\overline{SC2S'}$
	C4	A12	EF
	C5	K12	Indicator 29
Subcom 1 in	D15	C12	
Word 2	C13	A12	EF
	C11	J19	$\overline{2^4}$ W/F Counter
	C14	J16	Indicator 31
Subcom 2 in	B7	C5	
Word 8	B5	A12	EF
	B4	A20	Indicator 32
Gate 3	A14	J18	$\overline{2^3}$ W/F Counter
	A21	J20	$\overline{2^4}$
	A15	C16	Level for Word 8 only
Subcom 2 in	B9	C5	
Word 16	B12	A12	EF
	B11	J18	$\overline{2^3}$ W/F Counter
	B6	D6	Indicator 20
External Reset	A18	B18	$\overline{ER}$
Multiplex Inhibit	K6	A13	EF
Counter Reset	E13	K2	
Pulse, Gate 2	K1	A13	EF

Quick Look Patch Panel Wiring For S-17

Circuit and Function	Patch Panel Pins		Signals (Level or Pulse)	
	From	To		
Binary Register No. 1	U1	Z1	2^0	True
	U3	Z2	2^1	Shift Register
	U5	Z3	2^2	Outputs for
	.	.	.	Frame Sync
	.	.	.	Code
	.	.	.	
	.	.	.	
	U29	Z15	2^{14}	
	U31	Z16	2^{15}	
	U2	V1	$\overline{2^0}$	False Shift
	U4	V2	$\overline{2^1}$	Register
	.	.	.	Outputs
	.	.	.	for
	.	.	.	Frame
	U30	V15	$\overline{2^{14}}$	Sync
	U32	V16	$\overline{2^{15}}$	Code
	G1	J1	2^0	W/F
	G2	J3	2^1	Counter
	G3	J5	2^2	for word
	G4	J7	2^3	"32"
	G5	J9	2^4	
	G6	G23	EW	
Binary Register No. 2	T1	Z1		
	T2	V1	Shift Register	
	T3	V2	Outputs for	
	T4	Z2	Complementary	
	T5	Z3	Frame Sync	
	T6	V3	Code	
	T7	Z4		
	T8	V4		
	T9	V5		
	T10	Z5		
	T11	V6		
	T12	Z6		
	T13	Z7		
	T14	V7		
	T15	V8		
	T16	Z8		
	T17	Z9		
	T18	V9		
	T19	V10		
	T20	Z10		
	T21	V11		

Quick Look Patch Panel Wiring For S-17

Circuit and Function	Patch Panel Pins From	Patch Panel Pins To	Signals (Level or Pulse)
Binary Register No. 2	T22	Z11	Shift Register Outputs for Complementary Frame Sync Code
	T23	V12	
	T24	Z12	
	T25	V13	
	T26	Z13	
	T27	Z14	
	T28	V14	
	T29	Z15	
	T30	V15	
	T31	Z16	
	T32	V16	
	G12	J1	2^0 W/F Counter for word "32"
	G13	J3	2^1
	G14	J5	2^2
	G15	J7	2^3
	G16	J9	2^4
	G17	G23	EW
Binary/BCD Converter Control No. 1	S1	Z1	2^0 S. R. Output for SC Sync code verification (1111. . . .)
	S2	Z2	2^1
	.	.	.
	.	.	.
	.	.	.
Word B	S8	Z8	2^7
	S9 thru 16	S33	GROUND
Gate 7 & Gate 8	F1 & F12	J15	2^0 SC Counter 1 outputs for words "16" and "48"
	F2 & F13	J17	2^1
	F3 & F14	J19	2^2
	F4 & F15	J21	2^3
	F5 & F16	J24	$\overline{2^4}$
	F17	J25	2^5
	F6	J26	$\overline{25}$
	F7 & F18	G24	EW
	F8 & F19	B11	W/F Counter, Words 2 or 18
Gate 1	B1	J1	2^0 W/F Counter Outputs for words 2 & 18
	B2	J4	$\overline{2^1}$
	B3	J6	$\overline{2^2}$
	B4	J8	$\overline{2^3}$
Binary/BCD Converter No. 2 Word A	S17	Z1	Shift Register outputs for SC sync code (0101. . . .)
	S18	Z2	
	S19	Z3	
	S20	Z4	
	S21	Z5	
	S22	Z6	
	S23	Z7	
	S24	Z8	
	S25 thru S32	S33	GROUND

Error Monitor Patch Panel Wiring For S-17

Circuit and Function	Patch Panel Pins		Signals (Level or Pulse)			
	From	To				
Frame Sync Bit Error Shift Register	E1	K1	2^{0}	Shift Register Outputs (Complementary Frame sync code)	1	False Frame Sync Code
	E2	H2	$\overline{2^{1}}$		0	
	E3	K3	2^{2}		1	
	E4	K4	2^{3}		1	
	E5	H5	$\overline{2^{4}}$		0	
	E6	H6	$\overline{2^{5}}$		0	
	E7	K7	2^{6}		1	
	E8	H8	$\overline{2^{7}}$		0	
	E9	K9	2^{8}		1	
	E10	H10	$\overline{2^{9}}$		0	
	E11	H11	$\overline{2^{10}}$		0	
	E12	H12	$\overline{2^{11}}$		0	
	E13	H13	$\overline{2^{12}}$		0	
	E14	K14	2^{13}		1	
	E15	K15	2^{14}		1	
	E16	K16	2^{15}		1	
	D1 & D2 & D3 & D4 & .... & D16	C1	GROUND			

Patch Panel Wiring List For S-49

Search and Lock Patch Panel Wiring For S-49

Circuit and Function	Patch Panel Pins From	Patch Panel Pins To	Signals (Level or Pulse)			
Frame Sync	S1	V2	2^{0}		0	
Recognizer	S3	V3	2^{1}		1	
(In-phase)	S5	V6	2^{2}		0	
	S7	V7	2^{3}		1	
	S9	V9	2^{4}		1	
	S11	V12	2^{5}		0	
	S13	V13	2^{6}		1	
	S15	V16	2^{7}		0	
	N1	Q1	2^{8}		1	
	N3	Q4	2^{9}		0	
	N5	Q6	2^{10}		0	
	N7	Q8	2^{11}	Shift	0	True
	N9	Q9	2^{12}	Register	1	Frame
	N11	Q11	2^{13}	Outputs	1	Sync
	N13	Q13	2^{14}		1	Code
	N15	Q15	2^{15}		1	
	J1	L1	2^{16}		1	
	J3	L4	2^{17}		0	
	J5	L6	2^{18}		0	
	J7	L7	2^{19}		1	
	J9	L10	2^{20}		0	
	J11	L12	2^{21}		0	
	J13	L13	2^{22}		1	
	J15	L15	2^{23}		1	
	E1	G2	2^{24}		0	
	E3	G4	2^{25}		0	
	E5	G6	2^{26}		0	
	E7	K7	Ground			
	E9	K9	"			
	.	.	"			
	.	.	"			
	.	.	"			
	E15	K15	"			
	D4	C6	-6 vdc for 3 bit errors			

Search and Lock Patch Panel Wiring For S-49

Circuit and Function	Patch Panel Pins		Signals (Level or Pulse)
	From	To	
Frame Sync Recognizer (Out-of-phase)	S2	V1	$\overline{2^{0}}$ 1
	S4	V4	2^{1} 0
	S6	V5	$\overline{2^{2}}$ 1
	S8	V8	2^{3} 0
	S10	V10	2^{4} 0
	S12	V11	$\overline{2^{5}}$ 1
	S14	V14	2^{6} 0
	S16	V15	$\overline{2^{7}}$ 1
	N2	Q2	2^{8} 0
	N4	Q3	$\overline{2^{9}}$ 1
	N6	Q5	$\overline{2^{10}}$ 1
	N8	Q7	$\overline{2^{11}}$ Shift 1 False
	N10	Q10	2^{12} Register 0 Frame
	N12	Q12	2^{13} Outputs 0 Sync
	N14	Q14	2^{14} 0 Code
	N16	Q16	2^{15} 0
	J2	L2	2^{16} 0
	J4	L3	$\overline{2^{17}}$ 1
	J6	L5	$\overline{2^{18}}$ 1
	J8	L8	2^{19} 0
	J10	L9	$\overline{2^{20}}$ 1
	J12	L11	$\overline{2^{21}}$ 1
	J14	L14	2^{22} 0
	J16	L16	2^{23} 0
	E2	G1	$\overline{2^{24}}$ 1
	E4	G3	$\overline{2^{25}}$ 1
	E6	G5	$\overline{2^{26}}$ 1
	D10	C7	-6 vdc for 3 bit errors
Data Input	A1	C15	
Clock Input	D17	C17	Divide by 2 for NRZ
Frame Synchronization (In-phase)	V17	U18	$\overline{2^{0}}$ Lock Counter.
	V20	U20	2^{1} Locks after "3"
	V21	U22	$\overline{2^{2}}$ valid frames.
	T17	R18	$\overline{2^{0}}$ Search Counter
	T20	R20	2^{1} Flywheeling "7"
	T22	R22	2^{2} frames.
	T17	R17	Begins searching
	T19	R19	immediately.
	T21	R21	Search Counter
	T23	R23	
	C18	D18	Search Pulse for out-of-phase
	Q17	P17	FSW
	Q19	P19	FSW'

Search and Lock Patch Panel Wiring For S-49			
Circuit and Function	Patch Panel Pins		Signals (Level or Pulse)
	From	To	
Frame Synchro- nization (Out-of-phase)	Q21	P21	FS'
	Q23	P23	$\overline{\text{Frame Search}}$
	N17	M18	$\overline{2^0}$ Lock Counter.
	N20	M20	$\overline{2^1}$ Locks after "3"
	N21	M22	$\overline{2^2}$ valid frames.
	L17	K18	$\overline{2^0}$ Search Counter.
	L19	K20	$\overline{2^1}$ Begins searching
	L21	K22	2^2 immediately.
Word Sync (not used)	C21	D21	Disables word search
	C20	D19	and word lock.

B/W/F Counters Patch Panel Wiring For S-49

Circuit and Function	Patch Panel Pins From	Patch Panel Pins To	Signals (Level or Pulse)	
B/W Counter,	Y1	Z2	$\overline{2^0}$	To count 9
Establishing	Y2	Z4	$\overline{2^1}$	bits per word
Words, 9 bits	Y3	Z6	$\overline{2^2}$	"8"
per word	Y4	Z7	2^3	
	Y5	Z10	$\overline{2^4}$	
	U16	Y9 & U13	$\overline{FR}$	
	S16	Y10 & U14	$\overline{WFR}$	
W/F Counter,	W1	X1	2^0	
Establishing	W2	X3	2^1	To reset counter
Frames, 128 words	W3	X5	2^2	after 128 words,
per frame.	W4	X7	2^3	"127" and
	W5	X9	2^4	establish EF
Reset Gate	W6	X11	2^5	
	W7	X13	2^6	
Preset Gate	W8	X2	$\overline{2^0}$	To preset
	W9	X3	2^1	counter to "0"
	W10	X6	$\overline{2^2}$	at word 3
	W11	X8	$\overline{2^3}$	"2"
	W12	X10	$\overline{2^4}$	
	W13	X12	$\overline{2^5}$	
	W14	X14	$\overline{2^6}$	
W/F Counter	U1	V1 & Y11		Presets counter
Preset Gate	U2	V3		to "3"
	U3	V6		
	U4	V8		
	U5	V10		
	U6	V12		
	U7	V14		
Frames/Subcom	P14	Y13	To count frames	
Counter 1				
Preset Gate	S1	X2	$\overline{2^0}$	W/F Counter
	S2	X4	$\overline{2^1}$	outputs to
	S3	X6	$\overline{2^2}$	preset subcom
	S4	X8	$\overline{2^3}$	"64" counter
	S5	X10	$\overline{2^4}$	to 64 for
	S6	X12	$\overline{2^5}$	subcom count
	S7	X13	2^6	comparison
	S8	W16	EW	
	S14	C34	W64 to SC corrector	

B/W/F Counters Patch Panel Wiring For S-49

Circuit and Function	Patch Panel Pins From	Patch Panel Pins To	Signals (Level or Pulse)	
Preset Gate (Cont'd)	G16 & H16 & F16	Y16	C'	To disable subcom counters 2 & 3
	P16 & M16 & K16	Z17	Ground	
	D14 & J14	Y17	Ground	
Subcom Counter Corrector	F21	Z21	2^2	Shift Register outputs to check spacecraft subcom counter updating.
	F23	Z22	2^3	
	F25	Z23	2^4	
	F27	Z24	2^5	
	F29	Z25	2^6	
	F31	Z26	2^7	
	F33	Z27	2^8	
	F22	U21	$\overline{2^2}$	
	F24	U22	$\overline{2^3}$	
	.	.	.	
	.	.	.	
	.	.	.	
	F32	U26	$\overline{2^7}$	
	F34	U27	$\overline{2^8}$	
	E21	T1	2^0	Subcom Counter outputs to make comparison with S. R. outputs
	E23	T3	2^1	
	.	.	.	
	.	.	.	
	.	.	.	
	E31	T11	2^5	
	E33	T13	2^6	
	E22	T2	$\overline{2^0}$	
	E24	T4	$\overline{2^1}$	
	.	.	.	
	.	.	.	
	.	.	.	
	E32	T12	$\overline{2^5}$	
	E34	T14	$\overline{2^6}$	
	C27	C31		Flywheel Counter set to "6"
	C29	C30		
Frames/Subcom Counter 1	D21	Q1		To set counter
	D22	Q3		
	D23	Q5		
	.	.		
	.	.		
	.	.		
	D27	Q13		

B/W/F Counters Patch Panel Wiring For S-49			
Circuit and Function	Patch Panel Pins		Signals (Level or Pulse)
	From	To	
Frames/Subcom Counter 1 (Cont'd)	D28	Q2	To Reset Counter
	D29	Q4	
	.	.	
	.	.	
	.	.	
	D33	Q12	
	D34	Q14	
	G1 & M1	V16	EWL

Accumulator Patch Panel Wiring For S-49

Circuit and Function	Patch Panel Pins From	Patch Panel Pins To	Signals (Level or Pulse)
Data Present	G15 & G10	E18	EW
Counter:	H8	G11	2^0
	H9	G12	2^1
	G14	A7	DP, to be delayed
Gate 3:	A14	G13	$\overline{DP}$ Added
	A21	A16	$\overline{EF}$
	A15	D1 & K1	(DP & EF)
DMA27	K2	H14	Counter Reset
DMA25	K16	J14	DP delayed
Gate 2	E12	J12	$\overline{DP}$ delayed
	E13	A16	$\overline{EF}$
Gate 4	A23	E14	($\overline{DP}$ & $\overline{EF}$)
	A4	B1	(WFL) (DL)
	A6	K15	Data Present Pulse
Time Present	F7	A12	EF
	F6	B1	(WFL) (DL)
	E16	J2	$\overline{TP}$
Subcom Sync	E1	H18	2^0
Gate 1	E2	H20	2^1
	E3	H22	2^2 Subcom Counter 1 Word 127
	E4	H24	2^3
	E5	G19	2^4
	E6	G21	2^5
	E7	G23	2^6
	E8	J7	
Subcom Sync	J8	A12	EF
	J5	J6	
	J9	J4	
Flag 2	G7	B3	Subcom Sync
Dump, Flag 3	A8	B2	Dump
Frame Sync Quality Command	A10	A12	EF
Flag 4	A11	B20	$\overline{FSQ}$
FSQ Flag	D11	J12	$\overline{DP}$ to reset flip-flop
	C15	C18	CD to strobe FSQ
Subcom Sync Flag,	A3	J6	$\overline{SCS}$
Inverter 1	A5	K10	$\overline{SCS}$ for multiplexing
Multiplexing	B18	A18	$\overline{ER}$
	K5	A13	EF Enables multiplexing
	K6	G14	DP Disables multiplexing
	K7	K9	

Accumulator Patch Panel Wiring For S-49

Circuit and Function	Patch Panel Pins		Signals (Level or Pulse)
	From	To	
(WFL) (DL)	G17	D18	WFL
	H17	A13	EF
Data Register Expansion	D3	D4	Data Register Indicator Lights
	D5	D6	
	D7	D8	"
	D9	D10	"

Quick Look Patch Panel Wiring For S-49

Circuit and Function	Patch Panel Pins From	Patch Panel Pins To	Signal (Level or Pulse) S. R.		$\overline{\text{S. R.}}$	
Binary Register No. 1	U1	Z1	2^0			
	U2	V1			$\overline{2^0}$	
	U3	V2			$\overline{2^1}$	
	U4	Z2	2^1			
	U5	Z3	2^2			
	U6	V3			$\overline{2^2}$	
	U7	V4			$\overline{2^3}$	
	U8	Z4	2^3			
	U9	V5			$\overline{2^4}$	
	U10	Z5	2^4			
	U11	Z6	2^5			
	U12	V6			$\overline{2^5}$	
	U13	V7			.	
	U14	Z7	.	True		False
	U15	Z8	.	Shift		Shift
	U16	V8		Register	.	Register
	U17	V9		Outputs	.	Outputs
	U18	Z9	.			
	U19	Z10	.			
	U20	V10			.	
	U21	Z11	.			
	U22	V11			.	
	U23	Z12	.			
	U24	V12			.	
	U25	V13			.	
	U26	Z13	.			
	U27	V14			.	
	U28	Z14	.			
	U29	V15			.	
	U30	Z15	.			
	U31	V16			$\overline{2^{15}}$	
	U32	Z16	2^{15}			
	G1	J2	2^0			
	G2	J3	2^1	W/F Counter		
	G3	J6	2^2			
	G4	J8	2^3	outputs.		
	G5	J10	2^4			
	G6	J12	2^5			
	G7	J14	2^6	Sample at		
	G8	G23	EW Word "3"			

Quick Look Patch Panel Wiring For S-49

Circuit and Function	Patch Panel Pins From	Patch Panel Pins To	Signals (Level or Pulse)		
Binary Register No. 2			S. R.		$\overline{\text{S. R.}}$
	T1	V17			$\overline{2^{16}}$
	T2	Z17	2^{16}		
	T3	Z18	2^{17}		
	T4	V18			$\overline{2^{17}}$
	T5	Z19	2^{18}		
	T6	V19			$\overline{2^{18}}$
	T7	V20			$\overline{2^{19}}$
	T8	Z20	2^{19}		
	T9	Z21	.	Shift	
	T10	V21		Register	.
	T11	Z22	.	Outputs	
	T12	V22		of	.
	T13	V23	.	Frame	
	T14	Z23		Sync	.
	T15	V24	.	Code	
	T16	Z24			.
	T17	Z25	.		
	T18	V25			.
	T19	Z26	.		
	T20	V26			.
	T21	Z27	2^{26}		
	T22	V27			$\overline{2^{26}}$
	T23 & T25 & T27 & T29 & T31	Z34	GROUND		
	G12	J2	2^{0}	W/F Counter	
	G13	J3	2^{1}	Outputs	
	G14	J6	$\overline{2^{2}}$	to sample	
	G15	J8	$\overline{2^{3}}$	at word	
	G16	J10	$\overline{2^{4}}$	"3"	
	G17	J12	$\overline{2^{5}}$		
	G18	J14	$\overline{2^{6}}$		
	G19	G24	EW		

Quick Look - Decimal Display Patch Panel Wiring For S-49

Circuit and Function	Patch Panel Pins		Signals (Level or Pulse)	
	From	To		
Binary/BCD Converter Control No. 1 Word B	S1	Z3	2^2	Shift Register outputs (last 7 bits of word 65) of spacecraft subcom counter
	S2	Z4	2^3	
	S3	Z5	2^4	
	S4	Z6	2^5	
	S5	Z7	2^6	
	S6	Z8	2^7	
	S7	Z9	2^8	
	S8 & S9 & S10 &.. ... & S16	U34	GROUND	
Gate 7	F1	J2	$\overline{2^0}$	W/F Counter outputs for word "65"
	F2	J4	$\overline{2^1}$	
	F3	J6	$\overline{2^2}$	
	F4	J8	$\overline{2^3}$	
	F5	J10	$\overline{2^4}$	
	F6	J12	$\overline{2^5}$	
	F7	J13	2^6	
	F8	G25	EW	
Binary/BCD Converter Control No. 2, Word A	S17	Z1	2^0	S. R. Outputs of accumulated spacecraft time in words 33 and 34 (first 16 bits).
	S18	Z2	2^1	
	S19	Z3	2^2	
	.	.	.	
	.	.	.	
	.	.	.	
	S31	Z15	2^{14}	
	S32	Z16	2^{15}	
Gate 8	F12	J2	$\overline{2^0}$	W/F Counter outputs for word "35"
	F13	J3	2^1	
	F14	J6	$\overline{2^2}$	
	F15	J8	$\overline{2^3}$	
	F16	J10	$\overline{2^4}$	
	F17	J11	2^5	
	F18	J14	$\overline{2^6}$	
	F19	G26	EW	

Error Monitor Patch Panel Wiring For S-49

Circuit and Function	Patch Panel Pins From	Patch Panel Pins To	Signals (Level or Pulse)			
Frame Sync Bit	E1	K1	2^0		1	
Error Shift	E2	H2	2^1		0	
Register	E3	K3	2^2		1	
	E4	H4	2^3		0	
	E5	H5	2^4		0	
	E6	K6	2^5		1	
	E7	H7	2^6		0	
	E8	K8	2^7		1	
	E9	H9	2^8		0	
	E10	K10	2^9		1	
	E11	K11	2^{10}	Shift	1	
	E12	K12	2^{11}	Register	1	
	E13	H13	2^{12}	Outputs	0	
	E14	H14	2^{13}	(Comple-	0	False
	E15	H15	2^{14}	mentary	0	Frame
	E16	H16	2^{15}	Frame	0	Sync
	D1	G1	2^{16}	Sync	0	Code
	D2	J2	2^{17}	Code)	1	
	D3	J3	2^{18}		1	
	D4	G4	2^{19}		0	
	D5	J5	2^{20}		1	
	D6	J6	2^{21}		1	
	D7	G7	2^{22}		0	
	D8	G8	2^{23}		0	
	D9	J9	2^{24}		1	
	D10	J10	2^{25}		1	
	D11	J11	2^{26}		1	
	D12 & D13 & D14 & D15 & D16	C1	GROUND			

SECTION V

SPECIAL CIRCUITS

A. DIGITAL-TO-ANALOG ERROR DETECTOR

The digital-to-analog error detector, shown in figure V-1, is a programmable resistor summation and voltage divider network device used to generate an analog output signal voltage from a binary input. When the input terminals of the detector circuit are patched to a binary signal source, the output signal level varies inversely with the number of zero input signals present, and with the value of the programming resistor selected to couple the common summation junction (pin 24) to a reference source of -6 volts.

The circuit provides a signal of -2 VDC (minimum) at pin 20 whenever all diode inputs and R17 (pin 35) are at -6 VDC, or whenever the anticipated number of bad (positive) diode inputs is compensated for by applying -6 VDC to the equivalent "error resistor" (R18 through R22). The output signal cannot exceed 6 VDC, and will normally vary between -5 VDC and -2 VDC.

The digital-to-analog converter portion of the detector circuit consists of 32 precision resistors of equal value arranged in a ladder configuration to form a summation network. Sixteen of these resistors are mounted on card A, (figure V-2), while card B (figure V-3), contains the other 16 summation resistors, the six programming resistors, and two emitter-follower stages. The common junction of the summation and programming resistors is pin 24 of each card. This junction is coupled to the single output terminal (pin 20 of card B), by the complementary symmetry configuration of the NPN and PNP transistor emitter-followers.

B. OSCILLOGRAPH AMPLIFIERS

The oscillograph amplifier contains eight identical all-transistor galvanometer amplifiers mounted on a single printed circuit board. Each circuit used amplifies the signal from a digital-to-analog converter in the quick look unit to drive a galvanometer in the recording oscillograph. Figure V-4 is the schematic diagram for a typical amplifier circuit.

The input signal is fed through a level control to an emitter-follower which drives a pair of emitter-followers connected in the super alpha configuration. The return lead for the galvanometer coil is connected at the junction of the two 50-ohm resistors which are in series across the plus 6 and minus 6 volt sources. This protects the galvanometer by preventing the coil current from ever exceeding 100 ma. Zener diodes are used to regulate the plus 6 and minus 6 voltages.

C. DECIMAL DISPLAY CIRCUIT

The Decimal Display Circuit board (figure V-5), consists of a nixie indicator tube with separate transistor drivers for each of the ten cathodes. During the absence of input signals, the transistors are cut off and the indicator cathodes are at the same potential as the common plate. An input signal at the base of any transistor causes that transistor to conduct and thus drive the associated indicator cathode. This results in the display of a particular decimal digit.

D. FILTER BOARD

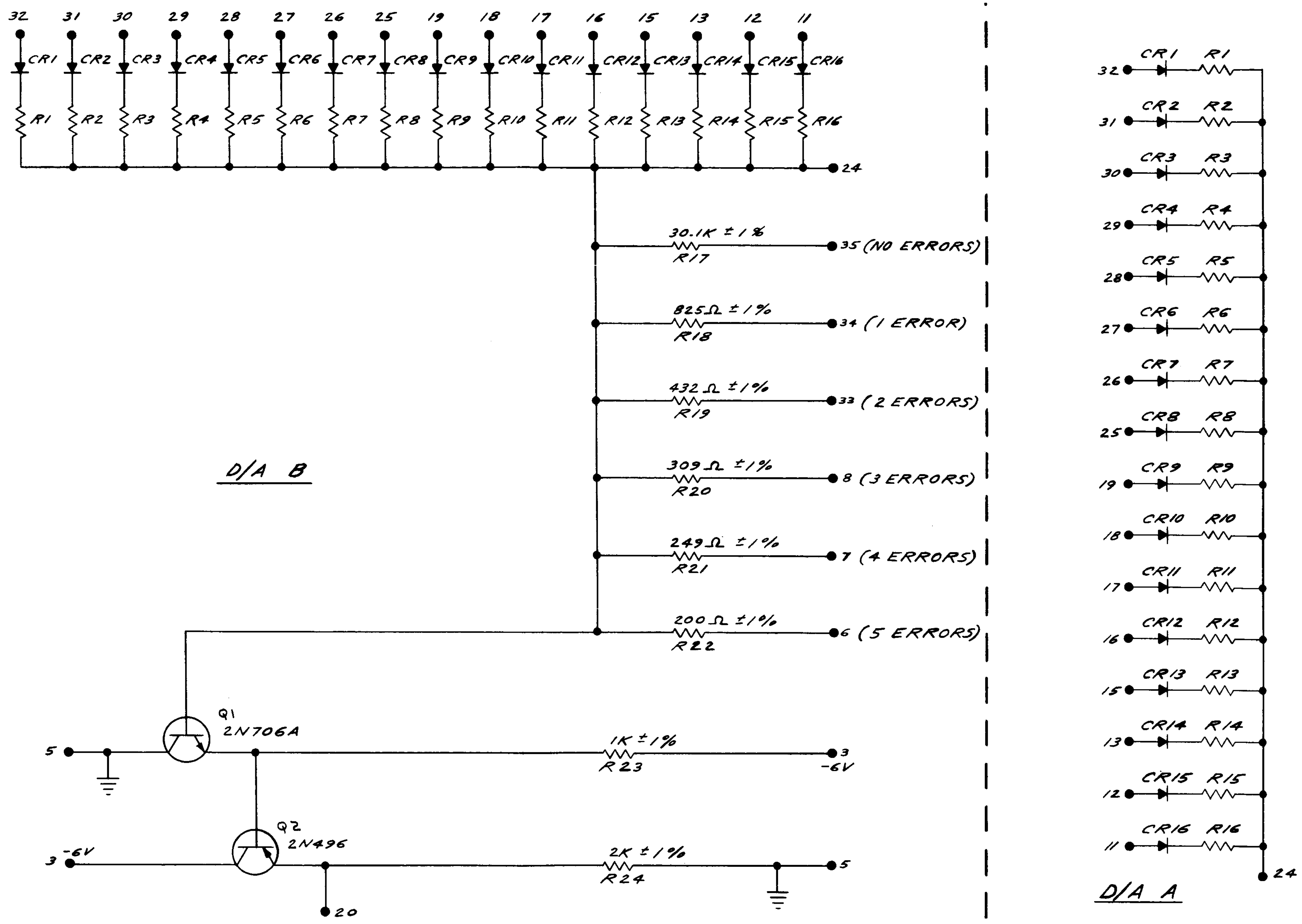
Cascade transistors, connected in an emitter-follower configuration, act as a buffer, or impedance matching device, between the input signal and the four filters (figure V-6). The filters, the inputs of which are connected in parallel, are hermetically sealed, band pass, telemetry filters. Each passes one of the four possible frequencies within its band pass, for which it is designed.

E. DRIVING CIRCUIT

The 0.4-KC driving circuit consists of a single-stage, linear, non-saturating, audio amplifier. This unit consists of a voltage amplifier, the output of which is applied to two emitter-followers connected in cascade. Also on this special card (figure V-7), are 1.6-KC, 7.2-KC, and 28.8-KC driving circuits which normally receive inputs from the filter board. These inputs are applied through r-c peak detector to the emitter-follower amplifier. As long as the detector capacitor remains charged, the emitter-follower is saturated, and an output is generated to subsequent circuitry.

F. BUZZER CIRCUIT

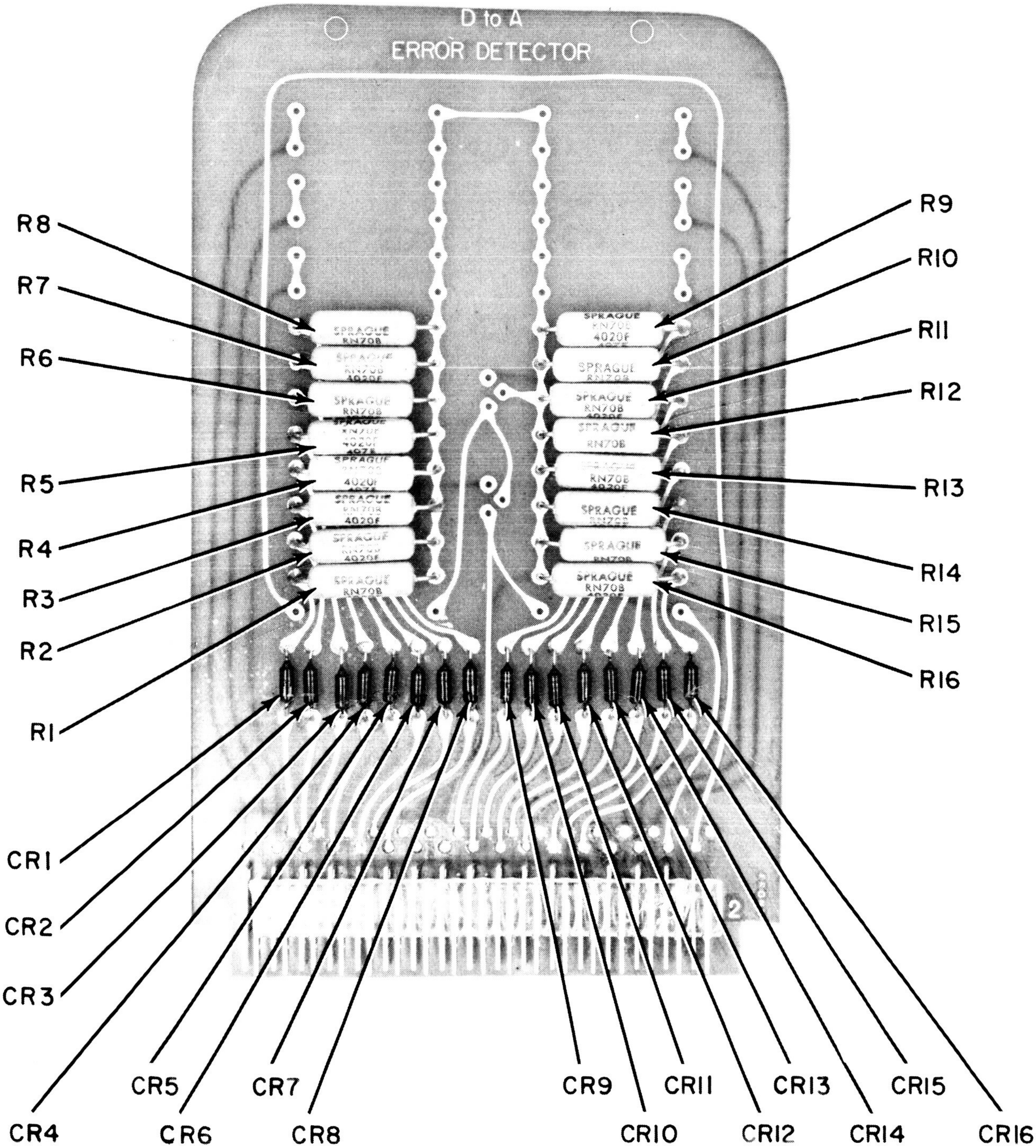
When ground (pin 8) is supplied to this module, the relay is energized, closing the normally open contacts. With the contacts closed, -6 VDC is applied to activate the buzzer.



NOTES:

1. ALL DIODES ARE IN251.
2. ALL RESISTORS ARE 402 OHMS ±1%, MIL-RN70, UNLESS OTHERWISE SPECIFIED.
3. ———● LOGIC CARD CONNECTOR PIN.
4. CIRCUITS A & B ARE ON SEPARATE 3C CARDS.

Figure V-1. Digital-to-Analog Error Detector



CIRCUIT A

Figure V-2. Error Detector A

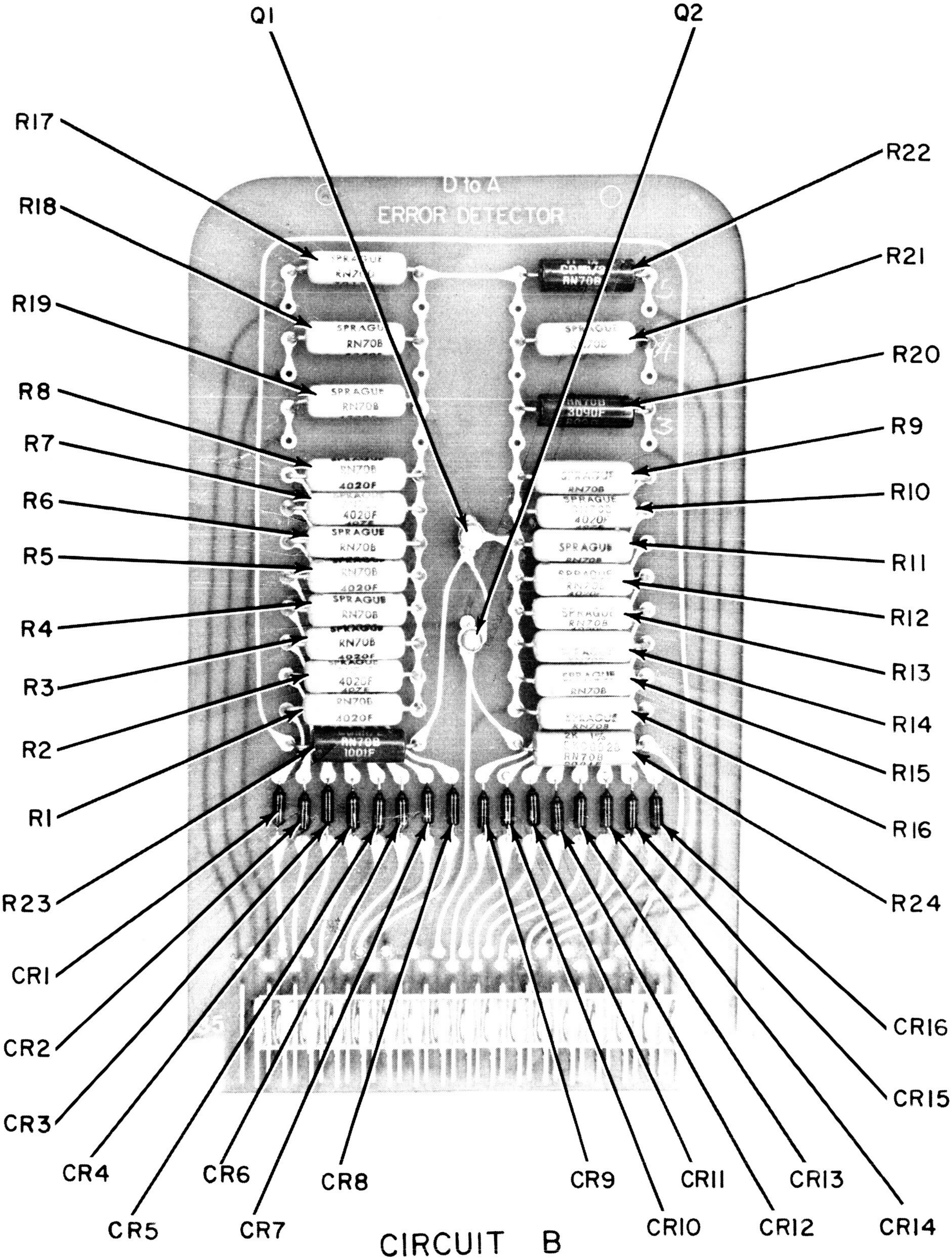


Figure V-3. Error Detector B

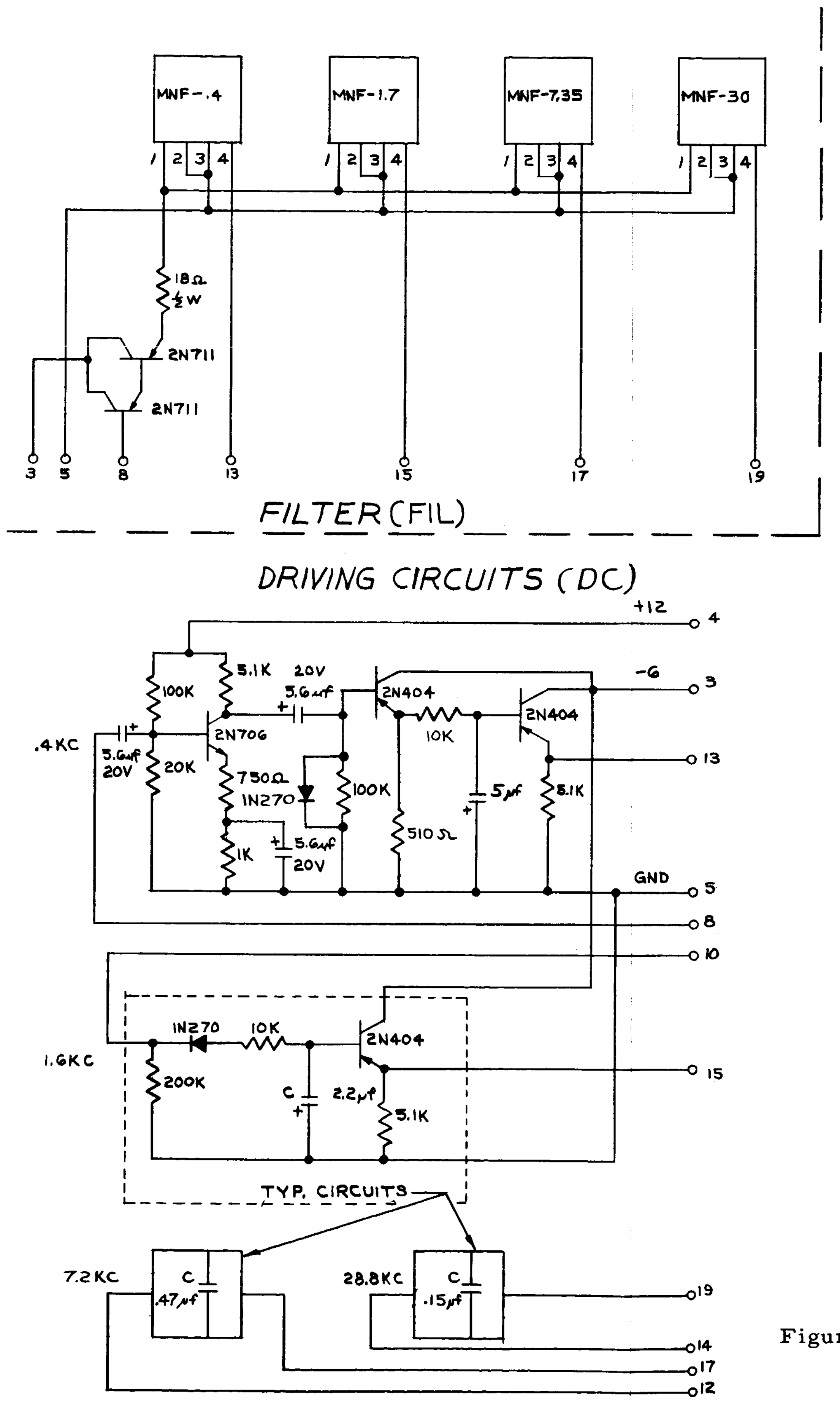
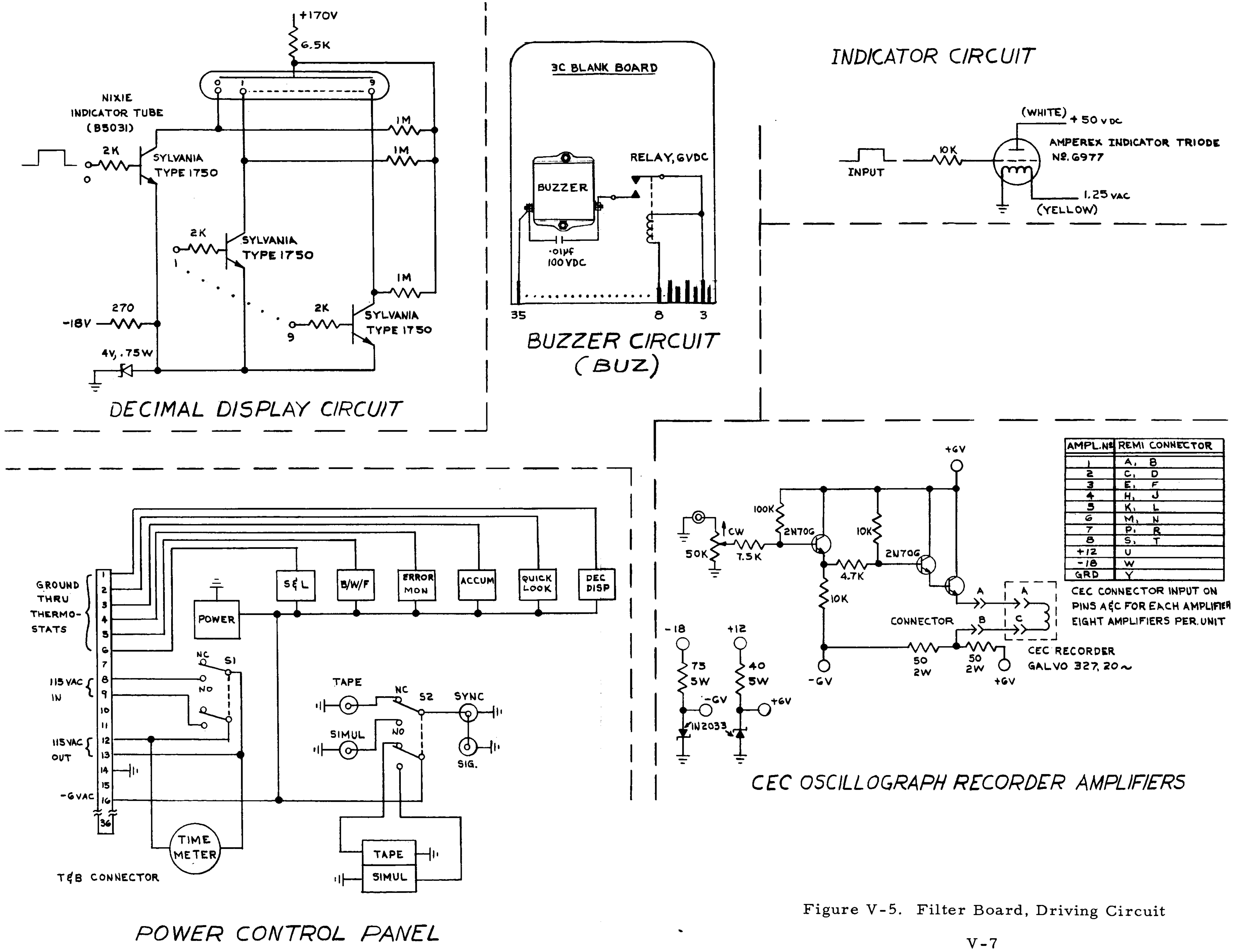


Figure V-4. Oscillograph Amplifier, Decimal Display Circuit



AMPL. No	REMI CONNECTOR
1	A, B
2	C, D
3	E, F
4	H, J
5	K, L
6	M, N
7	P, R
8	S, T
+12	U
-18	W
GRD	Y

Figure V-5. Filter Board, Driving Circuit

SECTION VI

SYSTEM ASSEMBLY AND WIRING

A. AC POWER DISTRIBUTION

Power switch S1 controls all direct line voltage to the three racks, except for the independent receptacles. When switch S1 is placed ON, 115 VAC is applied through the Thomas-Betts connector, energizing relay K1 in the rear (floor) of rack B (figure VI-1)*. The closing of the normally open contacts of relay K1 allow the 115-VAC line voltage through the circuit breaker and into the four power supplies mounted on the Rear Power Panel. These power supplies provide 170 VDC (PS1), 50 VDC (PS2), -10 VDC (PS3), and -6 VDC (PS4). In addition, transformer T1 is also connected in parallel with the four power supplies, providing 1.25 VAC.

With relay K1 energized, 115 VAC is also supplied to racks A and C, energizing similar K1 relays in the rear of these racks (figure VI-2)**. With these K1 relays energized, line voltage is supplied to the 50-VDC power supply (PS1) as well as the 1.25 VAC transformer (T1) on the Rear Power Panels located in each rack. Figures VI-3 and VI-4 illustrate the actual power distribution. Note that AC line voltage is routed to rack C (left) and rack A (right) via the large three-pronged connectors. AC voltage from rack B relay K1 contacts is applied to the K1 relay coils in rack C (left) and rack A (right) through the smaller two-pronged connectors.

Therefore, the power supplies in racks A and C each provide 50 VDC and 1.25 VAC. In rack A, these voltages are presently not used. The Signal Simulator Unit, Oscilloscope, and Oscillograph Recorder all utilize line voltage which is received via the K1 relays. The rack C equipment includes the Signal Synchronizer Unit, Search and Lock Unit, Data Accumulator Unit, and the Bits/Word/Frame Counters Unit.

All power obtained from the four power supplies and the transformer in rack B supply the units contained within rack B. The Decimal Display Unit receives 170 VDC; the Quick Look Monitor Unit receives 50 VDC, -10 VDC, and 1.25 VAC; the Error Monitor Unit also receives 50 VDC and 1.25 VAC; the Oscillograph Amplifiers receive +12 VDC and -18 VDC from Power Supply RP-32; Control and Indicator Panel receives -6 VDC, also from the RP-32 Power Supply in rack B.

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* Figure VI-3 pictorially depicts the location of components on the Rack B Rear Power Panel schematically illustrated in Figure VI-1.

** Figure VI-4 pictorially depicts the location of components on the Rack C Real Power Panel schematically illustrated in Figure VI-2.

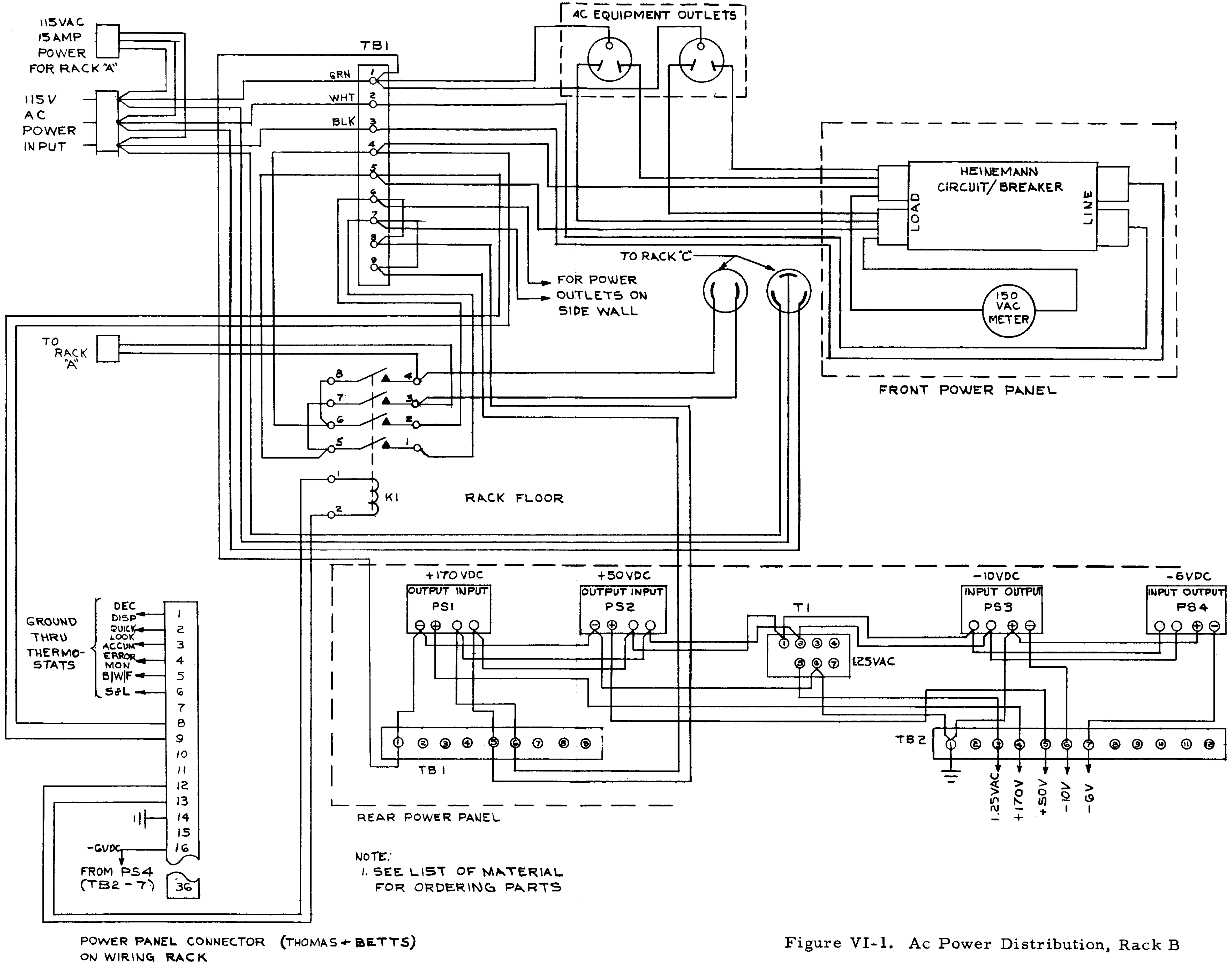


Figure VI-1. Ac Power Distribution, Rack B

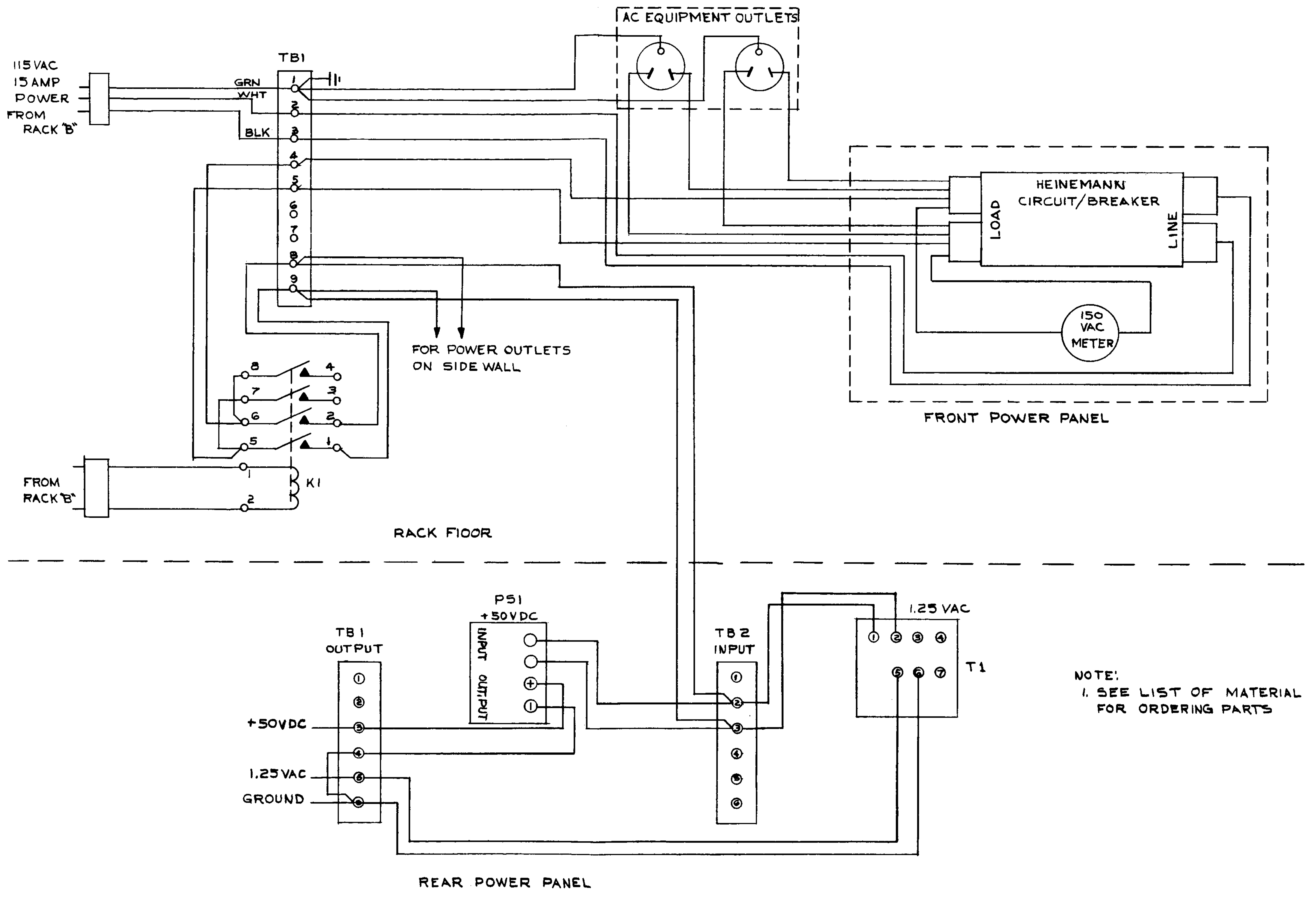


Figure VI-2. AC Power Distribution, Racks A and C

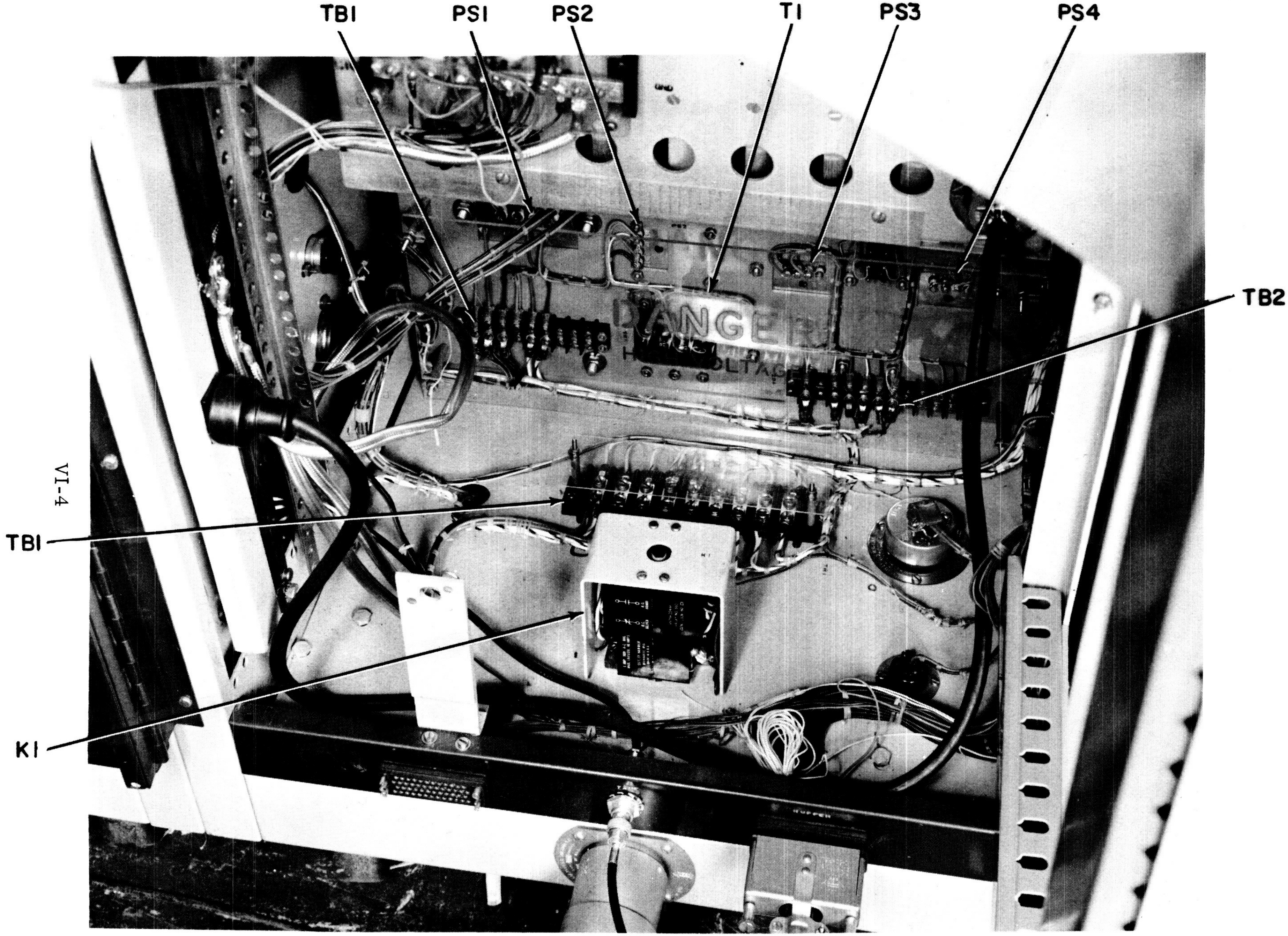


Figure VI-3. Rack B Rear Power Panel

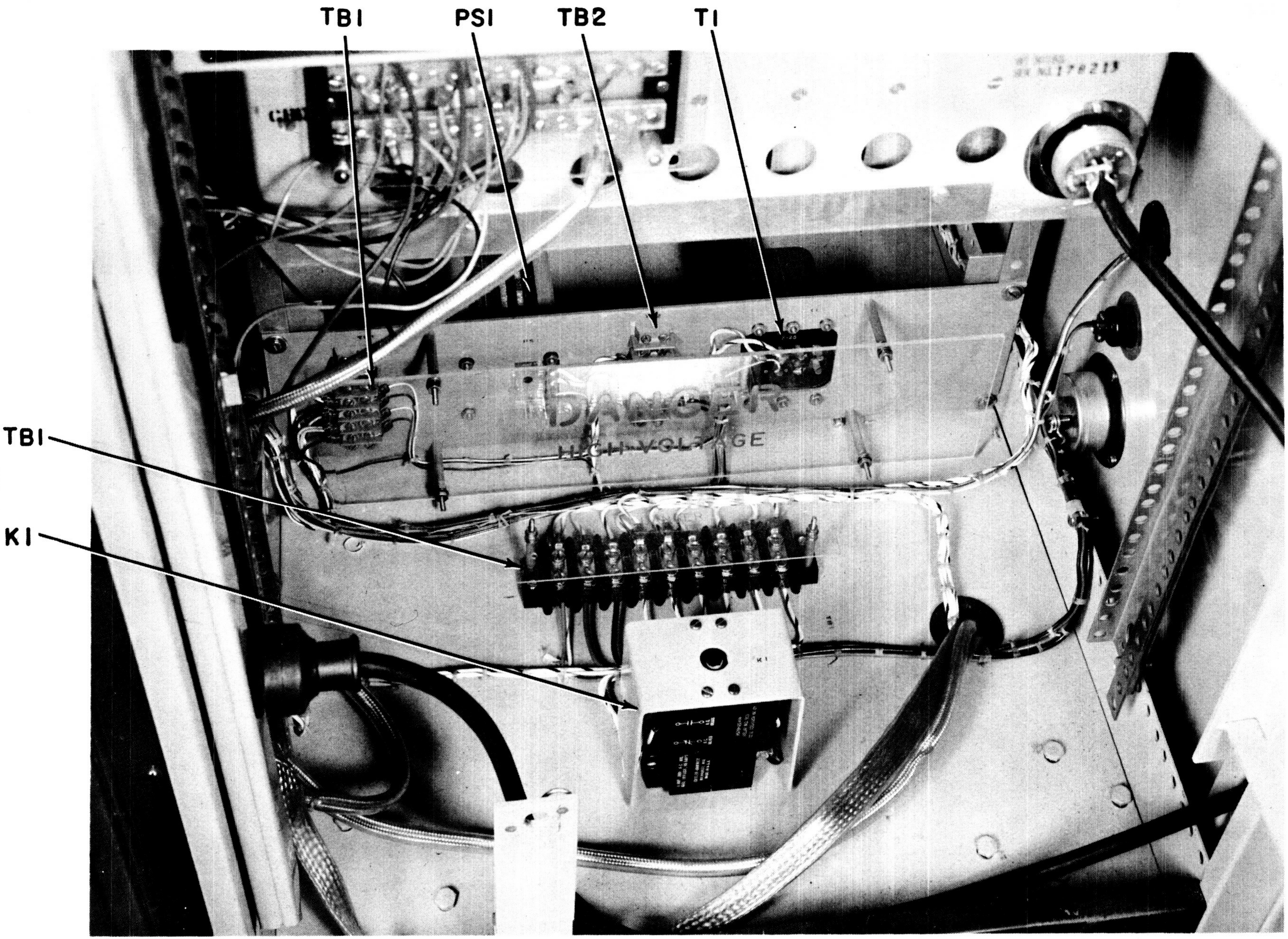


Figure VI-4. Rack C Rear Power Panel

B. SYSTEM PARTS LIST

The parts list for the PCM Data Processor is given in figure VI-5. Parts provided in this list are comprised of GSFC-built components as well as vendor components. This list is provided to aid in procuring the necessary component parts to maintain the equipment.

C. INTER UNIT WIRING

The three racks, as well as the units within each rack, are interconnected by either ribbon cable or cable harnesses. Some hard-wiring exists between racks, as indicated by the feed-through holes shown in figures VI-3 and VI-4. All units are interconnected in accordance with the interconnection wiring list, (figure VI-6). At the rear of each unit, a ribbon cable (flat) connects the chassis to its respective connectors on the rack door, whereupon cable harnesses interconnect each rack and other ribbon cable connectors within the same rack.

PART DESCRIPTION	TYPE OR PART NO.	QUANTITY PER SYSTEM	QUANTITY SPARES
RELAY, CUTLER - HAMMER	910	3	
CIRCUIT BREAKER, 115V, 15A HEINEMANN ELEC. CO.	XAM33	3	
TRANSFORMER, CHICAGO	F-25	2	
FAN, MUFFIN, ROTRON	C1A2	18	
POWER SUPPLY, 50.0-0.050A, TECHNIPOWER CO.		3	
POWER SUPPLY, 168.0-.375A, TECHNIPOWER CO.		1	
POWER SUPPLY, 9.8-1.5A, TECHNIPOWER CO.		1	
POWER SUPPLY, 6.9-1.5A, TECHNIPOWER CO.		1	
PATCH PATCH, AMP CONNECTORS CO.	695081-4	2	
PATCH BOARD, AMP CONNECTORS CO.	595005-1	2	
PATCH PANEL, AMP CONNECTORS CO.	695305-4	2	
PATCH BOARD, AMP CONNECTORS CO.	595350-1	2	
PATCH PANEL, AMP CONNECTORS CO.	595069-2	1	
PATCH BOARD, AMP CONNECTORS CO.	395056-1	1	
CONNECTOR, U.S. COMPONENTS	REMI 50 F2SL	8	
CONNECTOR, U.S. COMPONENTS	REMI 50 M2HRSL,	7	
CONNECTOR PIN, MALE, US COMPONENTS	1246-1	350	
CONNECTOR PIN, FEMALE, US COMPONENTS	1242-1	400	
BNC CONNECTOR, FEMALE	UG-492	20	
CONNECTOR & RIBBON, THOMAS & BETTS	PRC-PS 48	26	
CONNECTOR PIN, THOMAS & BETTS		1000	
CONNECTOR, HUBBELL	7466	5	
CONNECTOR	MS3102E-14S-6S	2	
CONNECTOR	MS3102E-14S-6P	2	
CONNECTOR, THOMAS & BETTS	35PFR-RS	36	
CONNECTOR, HUBBELL	525G	2	
CONNECTOR, HUBBELL	7465	2	
CONNECTOR, HUBBELL	7472	2	
CONNECTOR, HUBBELL	7328	2	
CONNECTOR, HUBBELL	7354	2	
CONNECTOR, HUBBELL	7958	1	
CONNECTOR, HUBBELL	7760	1	
SWITCH, PUSH BUTTON, SWITCHCRAFT CO.	933	5	
SWITCH, ROTARY, CENTRALAB CO.	2001	2	
LAMP, G.E.	345	10	
FUSE, 3AG, ¼A		5	
LIGHT INDICATOR W/LAMP (AMBER) NE2E, DIALCO	249-7841-93	5	
INDICATORS, PACKARD-BELL	L-50	10	
TRANSISTOR, SYLVANIA	1750	100	
DIODE	1N1507	20	
DIODE	1N595	20	
DIODE	1N270	5	
VOLT METER, 150 vac, 613 X 81, G.E.		3	
TIME METER, G.E.	50236402AAA	1	

PART DESCRIPTION	TYPE OR PART NO.	QUANTITY PER SYSTEM
TERMINAL STRIP, 9 POSITION, 9-150, CINCH-JONES		3
MICROSWITCH, SWITCHCRAFT CO.	2D26	6
INDICATOR	2C3	3
SCREEN	2A65	3
FILTER, RED	2G5	5
FILTER, GREEN	2G7	
BARRIER MOUNT	2B3	3
LOGIC CARDS, COMPUTER CONTROL COMPANY	BC 30	34
" " " " "	DM 30	11
" " " " "	FA 30	49
" " " " "	DN 30	43
" " " " "	DI 30	68
" " " " "	ST 30	6
" " " " "	DMA 30	4
" " " " "	PA 30	33
" " " " "	SR 30	24
" " " " "	IP 30	16
" " " " "	OD 30	10
" " " " "	MV 30	2
POWER SUPPLY, COMPUTER CONTROL COMPANY	RP 32	2
D/A, GSFC	GCURS1109830	10
FIL, GSFC	GCURS1110101	1
DC, GSFC	GCURS1110101	1
BUZ, GSFC	GCURS1110101	1
OSCIL. AMPL., GSFC	GCURS1110101	1

Figure VI-5. PCM System Parts List

1 FROM	2 TO	3 FUNCTION	4 DWG. №
S-1-1	E-1-1	SR-2^0	S-755
⋮	⋮	⋮	
S-1-32	E-1-32	SR-2^{31}	S-755
S-2-2	B-4-26	FSW	B-748
3	B-4-27	FSW′	B-748
4	A-5-1	WFL	S-759
5	B-4-29	$\overline{\text{WFR}}$	S-757
6	24	EW	B-747
7	25	EW′	B-747
8	B-4-28	$\overline{\text{WR}}$	S-758
9	B-4-31, E-6-14, D-1-35	$\overline{\text{ER}}$	S-754
10	B-4-21	$\overline{\text{C}}'$	S-753
11	E-6-1		
12	2		
13	3		
14	E-6-4	$\overline{\text{C}}'$	
15	B-4-20	C′	
16	B-4-23	$\overline{\text{CD}}$	
17	B-4 22	CD	
18	A-6-14	CD	S-753
19	B-4-30	$\overline{\text{FR}}$	S-759
20	B-4-32	SC SYNC	B-746
27	E-6-6	CD	S-753
S-2-35	A-6-35	DATA	S-753

1 FROM	2 TO	3 FUNCTION	DWG. №
E-4-1	Q-2-1	$\overline{\text{SR}}$-$\overline{2^0}$	E-765
⋮	⋮	⋮	
E-4-32	Q-2-32	$\overline{\text{SR}}$-$\overline{2^{31}}$	
E-5-1	Q-1-1	SR-2^0	
⋮	⋮	⋮	
E-5-32	Q-1-32	SR-2^{31}	E-765
E-6-4	E-6-5	$\overline{\text{C}}'$	S-753
-15	A-6-25	FSE	E-764
-16	-26		
-17	-27		
-18	-28		
E-6-19	A-6-29	FSE	E-764

1 FROM	2 TO	FUNCTION	DWG. №
Q-3-1	D-1-1	FOR DATA TO B/BCD, CONVERTER SHIFT REGISTERS.	
⋮	⋮		
-32	-32		
-33	33	GEW	Q-804
Q-3-34	D-1-34	GEW	Q-804

LEGEND

A-DATA ACCUMULATOR UNIT. E-ERROR MONITOR UNIT
B-B/W/F COUNTERS UNIT. Q-QUICK LOOK UNIT
D-DECIMAL DISPLAY UNIT S-SEARCH AND LOCK UNIT

COLUMNS 1 AND 2

A — 5 — 1 ← PIN OF CABLE CONNECTOR.
UNIT, CABLE CONNECTOR

COLUMN 3: SIGNAL FUNCTION
COLUMN 4: SOURCE OF SIGNAL
(THESE ARE THE LAST 3 DIGITS OF THE DWG. №)

1 FROM	2 TO		3 FUNCTION	4 DWG. №
A-4-1	BUFFER-A		2^0	A-769
2		B	2^1	
3		C	2^2	
4		D	2^3	
5		E	2^4	
6		F	2^5	
7		H	2^6	
8		J	2^7	
9		K	2^8	
10		L	2^9	
11		M	2^{10}	
12		N	2^{11}	
13		R	2^{12}	
14		S	2^{13}	
15		T	2^{14}	
16		U	2^{15}	
17		P	2^{16}	
18		V	2^{17}	A-769
21		c	DP	770
22		d	TP	
23		Y	FL1	
24		f	FL2	
25		h	FL3	
26		J	FL4	770
27		K	2^{18}	769
28		m	2^{19}	
29		n	2^{20}	
30		p	2^{21}	
31		s	2^{22}	
32		t	2^{23}	
33		r	2^{24}	
34		v	2^{25}	
A-4-35	BUFFER-z		2^{26}	769
A-5-1	B-5-29		WFL	S-759
A-6-1	BUFFER-u		FSQ	770
2		y	2^{27}	769
3		CC	2^{28}	
4		HH	2^{29}	
5		w	2^{30}	
6		AA	2^{31}	769
7		EE		770
8		-x		770
9		BB	SPARE	
10	BUFFER-FF.		DP INHIBIT	
11				
12				
13	B-4-32		SCS	B-746
A-6-18	B-4-31		$\overline{\text{ER}}$	S-754
A-6-36	S-2-29		$\overline{\text{(DL)(WFL)}}$	A-768

NOTE:
BUFFER CONNECTOR, PIN W IS SPARE.

1 FROM	2 TO	3 FUNCTION	4 DWG. №
A-6-16	E-6-10	FSE	F-764
17	BUFFER-DD	GRD	
18	a		
19	e		
20	z	STOP	
A-6-30	BUFFER-X		
FROM	TO	FUNCTION	DWG. №
E-3-1	B-1-1, A-1-1	SR-2^0	E-765
⋮	⋮ ⋮	⋮	
E-3-32	B-1-32, A-1-32	SR-2^{31}	
E-2-1	B-2-1, A-2-1	$\overline{\text{SR}}$-$\overline{2^0}$	
⋮	⋮ ⋮	⋮	
E-2-32	B-2-32, A-2-32	$\overline{\text{SR}}$-$\overline{2^{31}}$	E-765
B-3-1	A-3-1	W/F-2^0	B-748
2	2	W/F-$\overline{2^0}$	
⋮	⋮		
13	13	W/F-2^6	
14	A-3-14	$\overline{\text{W/F}}$-$\overline{2^6}$	
15	Q-4-1	W/F-2^0	
16	2	$\overline{\text{W/F}}$-$\overline{2^0}$	
⋮	⋮		
27	13	W/F-2^6	
28	Q-4-14	$\overline{\text{W/F}}$-$\overline{2^6}$	
29	A-5-3	EF	
B-3-30	E-6-9	EF	B-748
B-4-1	A-3-15, Q-4-15	SC1-2^0	B-745
2	16, Q-4-16	$\overline{\text{SC1-}2^0}$	
⋮	⋮ ⋮		
13	27, Q-4-27	SC1-2^6	
14	A-3-28, Q-4-28	$\overline{\text{SC1-}2^6}$	
15	A-5-4	$\overline{\text{SC1S}}'$	
16	-5	$\overline{\text{SC1S}}$	B-745
B-5-1	-11, Q-5-1	SC2-2^0	B-744
2	-12, Q-5-2	$\overline{\text{SC2-}2^0}$	
⋮	⋮ ⋮		
12	-22, Q-5-12	$\overline{\text{SC2-}2^5}$	
13	-6	$\overline{\text{SC2S}}'$	B-744
14	-7	$\overline{\text{SC2S}}$	
15	-23, Q-5-13	SC3-2^0	
16	-24, Q-5-14	$\overline{\text{SC3-}2^0}$	
⋮	⋮ ⋮		
26	-34, Q-5-24	$\overline{\text{SC3-}2^5}$	
27	-8	$\overline{\text{SC3S}}'$	
28	-9	$\overline{\text{SC3S}}$	B-744
30	A-5-2, E-6-8	$\overline{\text{EW}}$	B-747
31	Q-3-35	$\overline{\text{EW}}$	B-747
B-5-32	E-6-7	$\overline{\text{FSW}}$	B-748

Figure VI-6. Interconnecting Wiring List

SEARCH & LOCK

SLOT & CONNECTOR	BLOCK I	BLOCK II	BLOCK III
2			DI
3	BC	BC	DI
4	DM	DM	DI
5	BC	BC	DM
6	FA	FA	DMA
7	DN	DN	FA
8	DN	DN	PA
9	DI	DI	PA
10	DI	DI	PA
11			SR
12			SR
13	BC	DI	SR
14	DM	DI	SR
15	BC	DI	SR
16	FA	DI	SR
17	DN	DI	SR
18	DN	DI	SR
19	DI	DI	DN
20	DI	DI	DN
21		DI	DN
22		D/A *	ST
23		D/A *	
24		D/A *	
25		D/A *	
26		ST	
27			

ACCUMULATOR

SLOT & CONNECTOR	BLOCK I	BLOCK II	BLOCK III
2		DI	
3	FA	DI	
4	FA	DI	
5	FA	FIL *	
6	FA		
7	FA	DC *	
8	FA		
9	FA	ST	
10	DN	ST	
11	DI	DI	
12	PA	DM	
13	FA	FA	
14	FA	PA	
15	FA	DI	
16	DN	DI	
17	DM	DI	
18	DM	DI	
19	DN	PA	
20	BC	PA	
21	BC		
22	DI		
23	FA		
24	FA		
25	DMA	BUZ *	
26	DMA		
27	DMA		

BITS/WORD/FRAME COUNTERS

SLOT & CONNECTOR	BLOCK I	BLOCK II	BLOCK III
2			
3			
4	BC	BC	DI
5	BC	DI	DI
6	DN	BC	DI
7	DI	DI	DI
8	DN	DN	D/A *
9	DI	DN	D/A *
10	FA	FA	ST
11	BC	DN	D/A *
12	BC	DN	D/A *
13	PA	BC	DI
14	PA	DI	DI
15	PA	BC	DI
16	PA	DI	DI
17	D/A *	BC	DI
18	D/A *	DI	ST
19	DI	BC	
20	DI	DI	
21	DI	DN	
22	DI	DN	
23	DI	FA	
24	DN	FA	
25	BC		
26			
27			

DECIMAL DISPLAY

SLOT & CONNECTOR	BLOCK I	BLOCK II	BLOCK III
2			FA
3	OD	OD	MV
4	DN	DN	BC
5	DN	DN	PA
6	BC	BC	DN
7	OD	OD	DI
8	DN	DN	DI
9	DN	DN	DI
10	BC	BC	SR
11	OD	OD	SR
12	DN	DN	SR
13	DN	DN	SR
14	BC	BC	DM
15	OD	OD	FA
16	DN	DN	MV
17	DN	DN	BC
18	BC	BC	PA
19	OD	OD	DN
20	DN	DN	DI
21	DN	DN	DI
22	BC	BC	DI
23	DM	DM	SR
24		DM	SR
25			SR
26			SR
27			

* SPECIAL CIRCUIT ON 3C CARD.

NOTES:
1. ALL 3C CARDS ARE OF THE "-30" TYPE.

QUICK LOOK

SLOT & CONNECTOR	BLOCK I	BLOCK II	BLOCK III
2	LP	LP	
3	LP	LP	
4	FA	FA	
5	FA	FA	
6	LP	PA	
7	LP	DI	
8	FA	LP	
9	FA	LP	
10	PA	FA	
11	DI	FA	
12	LP	LP	
13	LP	LP	
14	FA	FA	
15	FA	FA	
16	LP	DI	
17	LP	DI	
18	FA	FA	
19	FA	FA	
20	LP	FA	
21	LP	FA	
22	FA	PA	
23	FA	DI	
24	PA	FA	
25	DI	FA	
26		FA	
27		FA	

ERROR MONITOR

SLOT & CONNECTOR	BLOCK I	BLOCK II	BLOCK III
2			
3			
4	SR	PA	
5	SR	PA	
6	DI	PA	
7	SR	PA	
8	SR	PA	
9	DI	PA	
10	SR	PA	
11	SR	PA	
12	DI	PA	
13	SR	PA	
14	SR	PA	
15	DI	PA	
16	PA	PA	
17		PA	DI
18		PA	BC
19	FA	PA	FA
20	DI	PA	
21	BC		
22			BC
23			
24			
25			
26			
27			

POWER CONNECTIONS FOR LOGIC CIRCUITS-
ALL UNITS: 3C POWER CONNECTOR (MS3106B14S-6P)

PIN	VOLTAGE (dc)
A	-18
B	-6
C	+12
D	GRD

POWER CONNECTIONS FOR INDICATORS-
SEARCH & LOCK, ACCUMULATOR, B/W/F COUNTERS, ERROR MONITOR UNIT: INDICATOR POWER CONNECTOR (MS3106B14S-6S)

PIN	VOLTAGE
A	+50 Vdc
B	1.25 Vac
C	GRD

DECIMAL DISPLAY UNIT: INDICATOR POWER CONNECTOR

PIN	VOLTAGE
F	+170 Vdc
C	GRD

QUICK LOOK UNIT: INDICATOR POWER CONNECTOR

PIN	VOLTAGE
A	+50 Vdc
B	1.25 Vac
F	-10 Vdc
C	GRD

ALL LOGIC CARD (3C) CONNECTORS IN ALL UNITS SHALL HAVE POWER CONNECTED AS FOLLOWS:

PIN	2,	3,	4,	5
VOLTAGE (dc)	-18,	-6,	+12,	GRD

POWER CONNECTOR FOR SYNCHRONIZER UNIT:
POWER CONNECTOR (K03-16-10SN)

PIN	VOLTAGE (dc)
A	-20
K	+20
L	-12
H	GRD

Figure VI-7. Location of circuit boards and DC Power connections

LIST OF APPLICABLE DRAWINGS

NOTE: All Drawing Numbers are prefixed by "CC-URS-"

Search & Lock Unit:

Strobe Generator & Data Polarity Inverter	1109753
Word Sync Recognizer & Reset Circuit	1109754
Serial-to-Parallel Converter	1109755
Frame Sync Recognizer	1109756
Frame or Word Sync (Øout)	1109757
Word Sync (Ø in)	1109758
Frame Sync (Ø in)	1109759

Bits/Word/Frame Counters Unit:

Subcom Sync Pattern Recognizer 3	1109740
Subcom Sync Pattern Recognizer 2	1109741
Subcom Sync Pattern Recognizer 1	1109742
Subcom Counter 3	1109743
Subcom Counter 2	1109744
Subcom Counter 1	1109745
Subcom Counter Corrector	1109746
Bits/Word Counter	1109747
Words/Frame Counter	1109748

Error Monitor Unit:

Frame Sync & Parity Error Indicator	1109764
S.R. Output Power Amplifiers	1109765
Frame Sync Error S.R.	1109766

Accumulator Unit:

Buffer Commands and Flags	1109770
Filter and Buffer Output Circuits	1109769
Buffer Data Register	1109768
Counter and Commands Circuits	1109767

Decimal Display Unit:

Binary/BCD Converter Control	1109773
Binary/BCD Converter 1, Decade 1	1109774
Binary/BCD Converter 1, Decade 2	1109775
Binary/BCD Converter 1, Decade 3	1109776
Binary/BCD Converter 1, Decade 4	1109777
Binary/BCD Converter 1, Decade 5	1109778
Binary/BCD Converter Control 2	1109779
Binary/BCD Converter 2, Decade 1	1109780
Binary/BCD Converter 2, Decade 2	1109781
Binary/BCD Converter 2, Decade 3	1109782
Binary/BCD Converter 2, Decade 4	1109783
Binary/BCD Converter 2, Decade 5	1109784

Quick Look Unit:

D/A Converter 1 & 2	1109581
D/A Converter 3 & 4	1109582
D/A Converter 5 & 6	1109583
D/A Converter 7 & 8	1109584
Binary Register 1	1109585
Binary Register 2	1109586
Auxiliary Gates	1109804

Special Drawings:

Definition of Symbols	1109730
Interconnection of Units, Wiring List	1110100
Special Circuits	1110101
Location of Cards and Power Connections In the System Units	1110102
Power Wiring, Rack A & C	1110103
Power Wiring, Rack B	1110104
Digital/Analog Converter & Detector	1109830

MANUALS

Synchronizer Unit: (Telemetrics, Inc.)

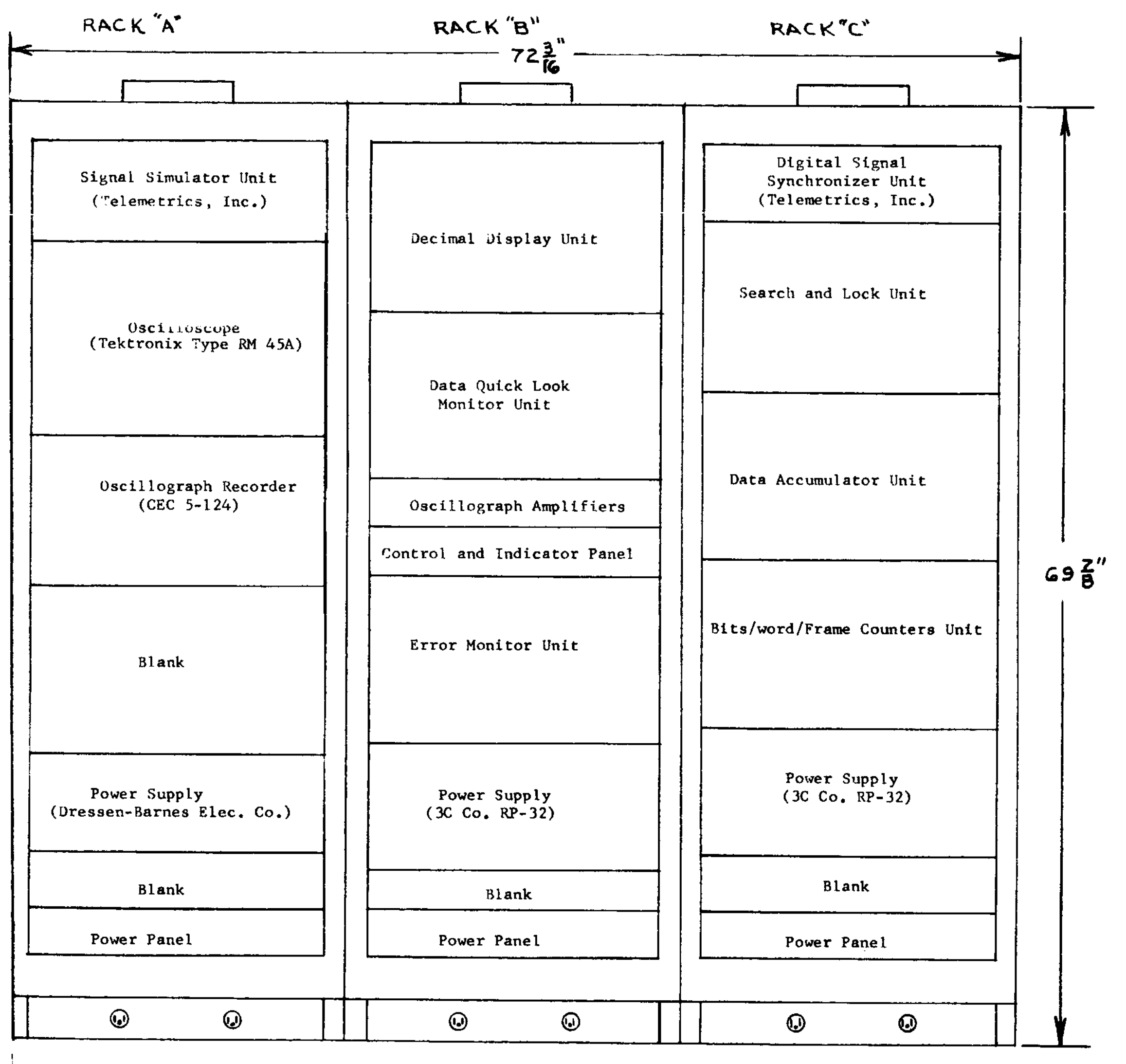
Operating And Instruction Manual For Digital Signal Synchronizer, Model 6103B

Simulator Unit: (Telemetrics, Inc.)

Operating And Instruction Manual For Digital Signal Simulator, Model ESS-503

Recording Oscillograph: (CEC)

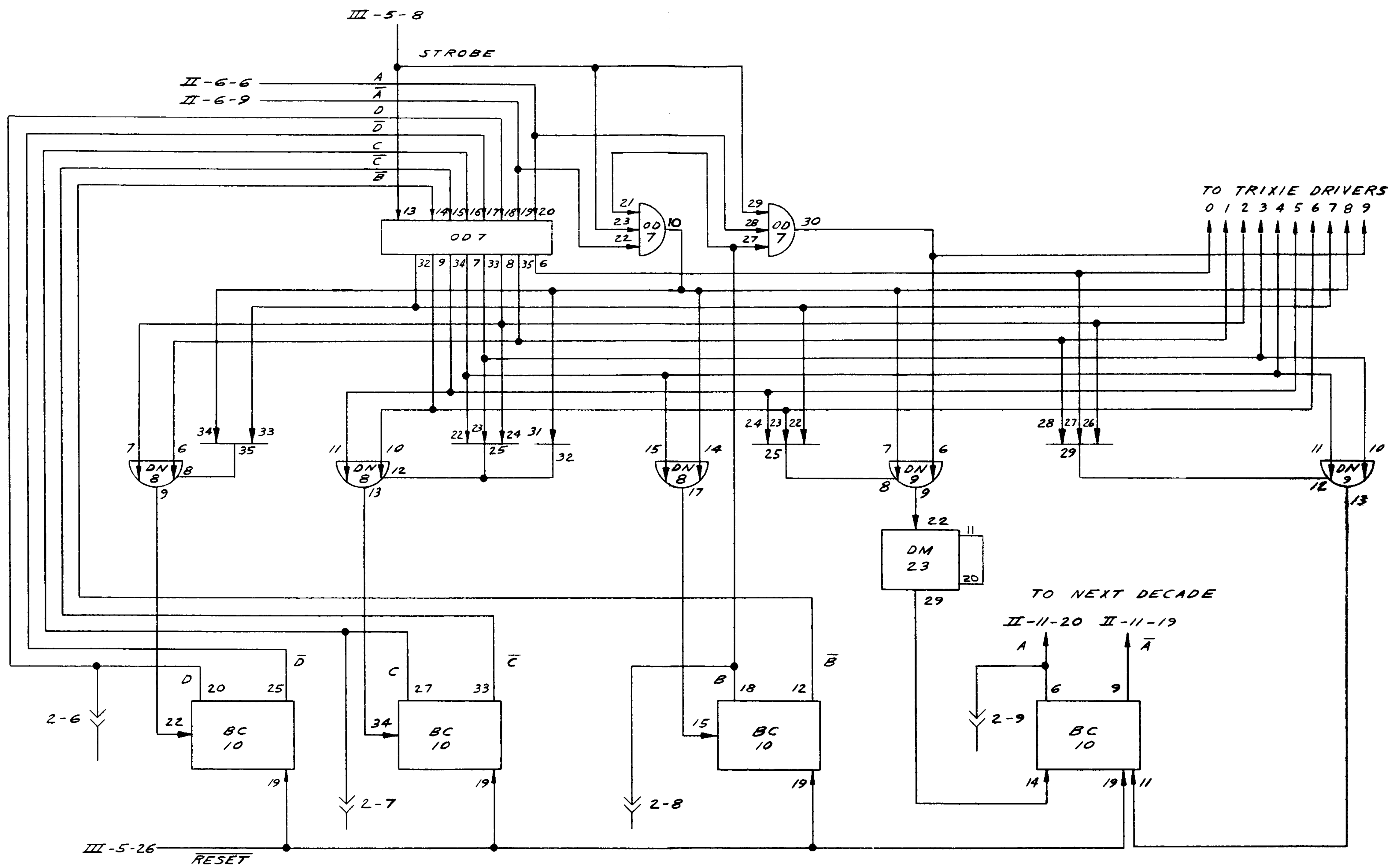
Operation and Maintenance Manual For Recording Oscillograph, Type 5-124



NOTES:

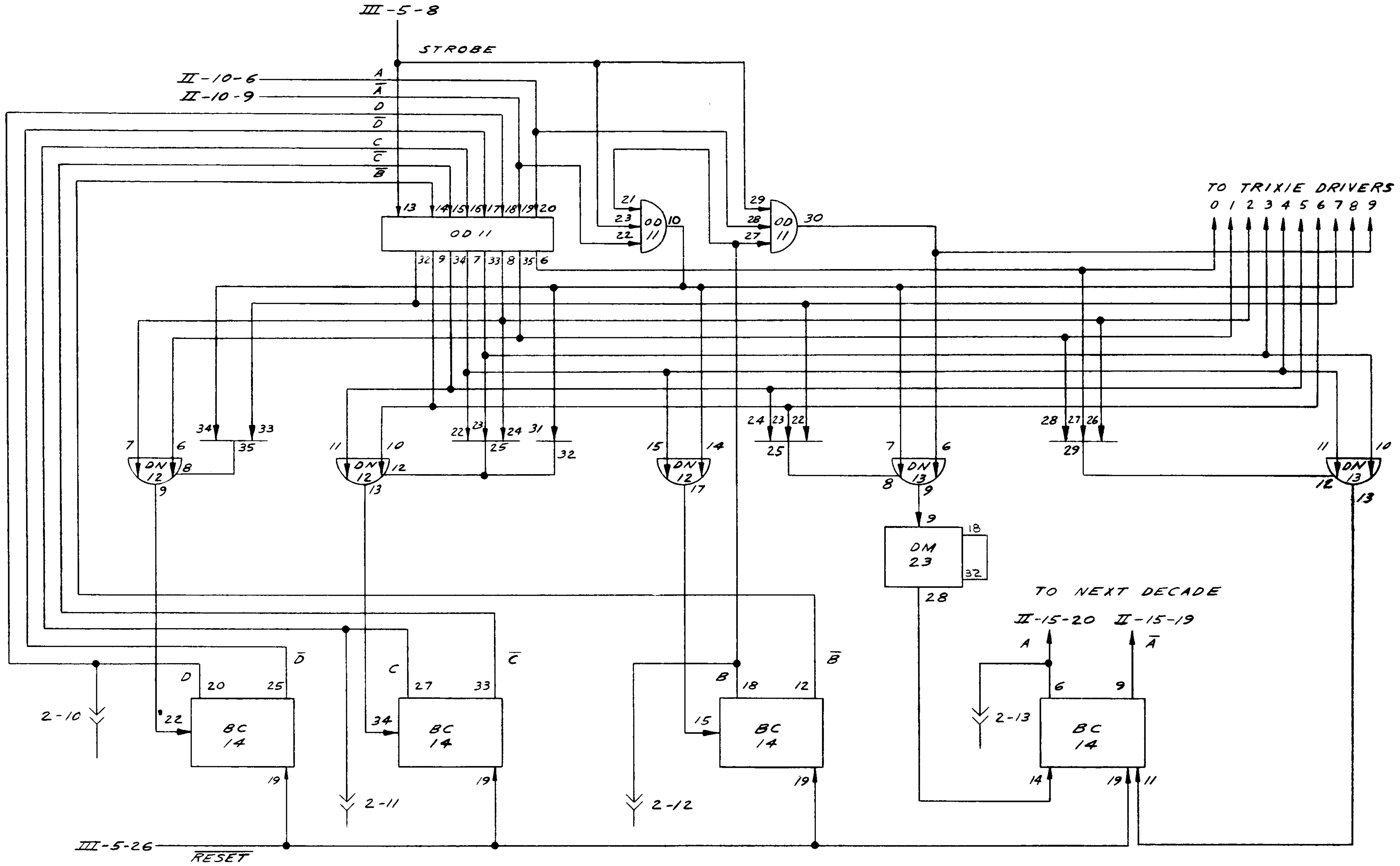
1. See Parts List (Dwg. No. 1110105) for parts mounted in the cabinets
2. Cabinets manufactured by EMCO

Figure VI-8. Location of System Units



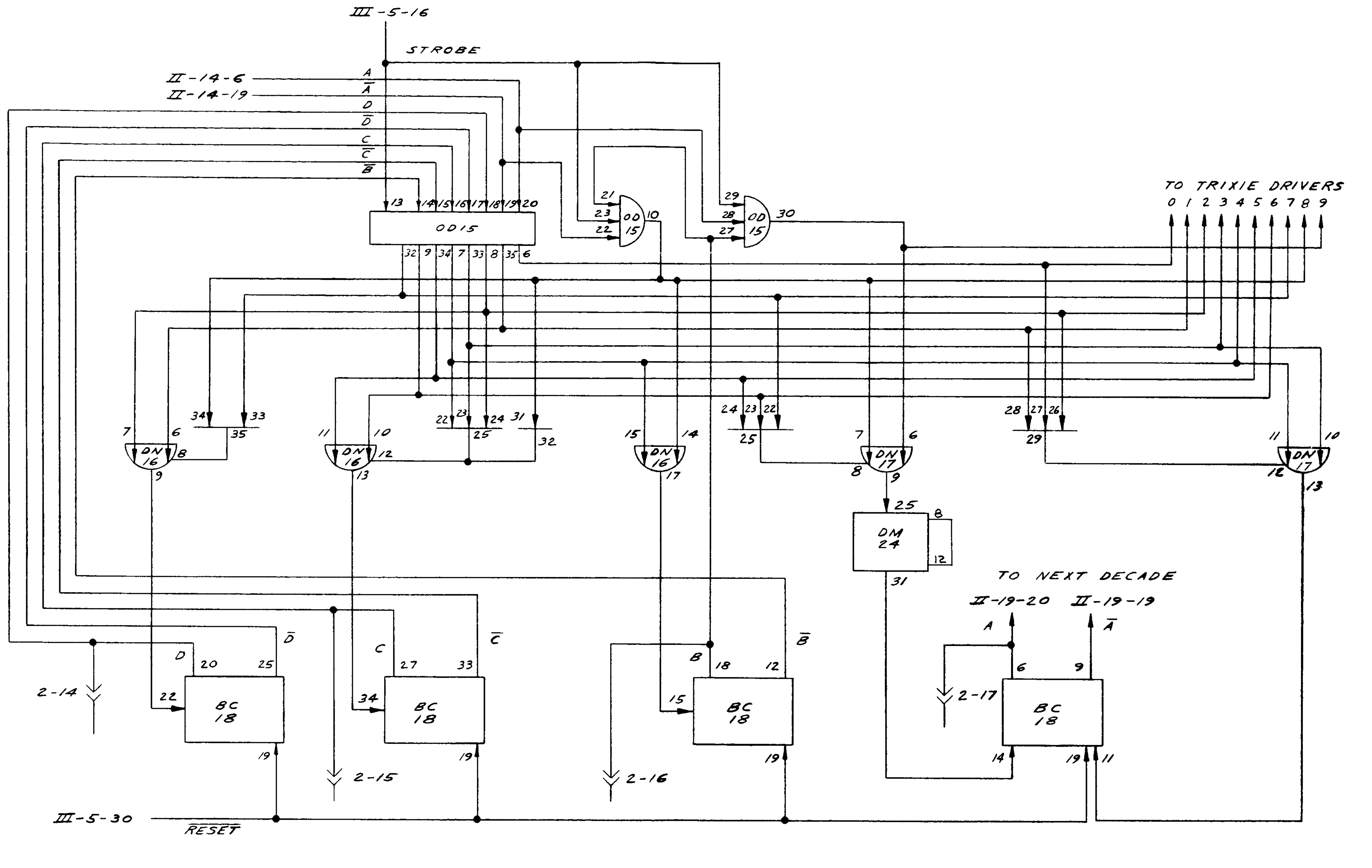
NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.

Figure VI-9. Decimal Display Unit, Binary/BCD Converter 1, Decade 2 (S-Block II)



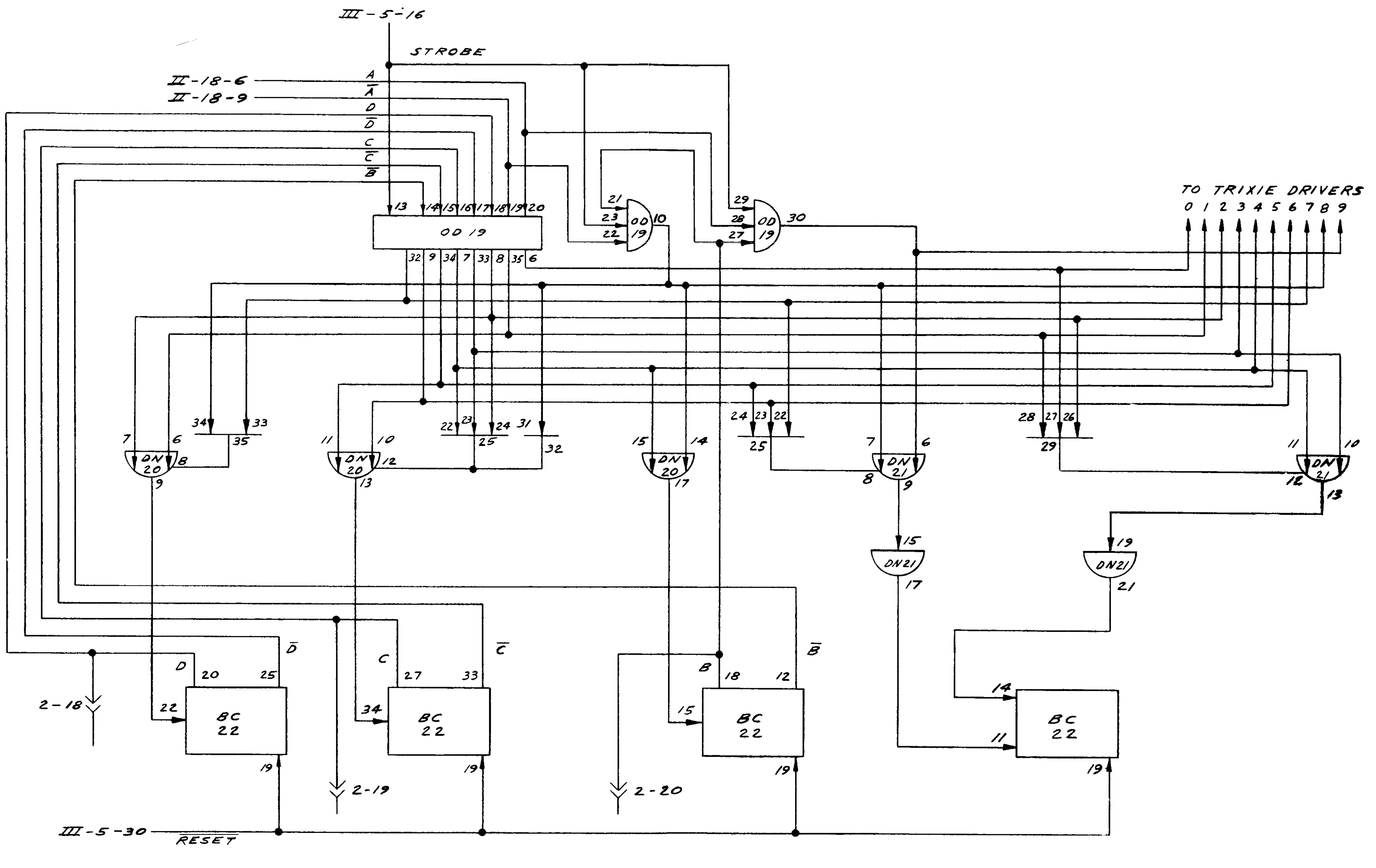
NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.

Figure VI-10. Decimal Display Unit, Binary/BCD Converter 1, Decade 3 (S-Block II)



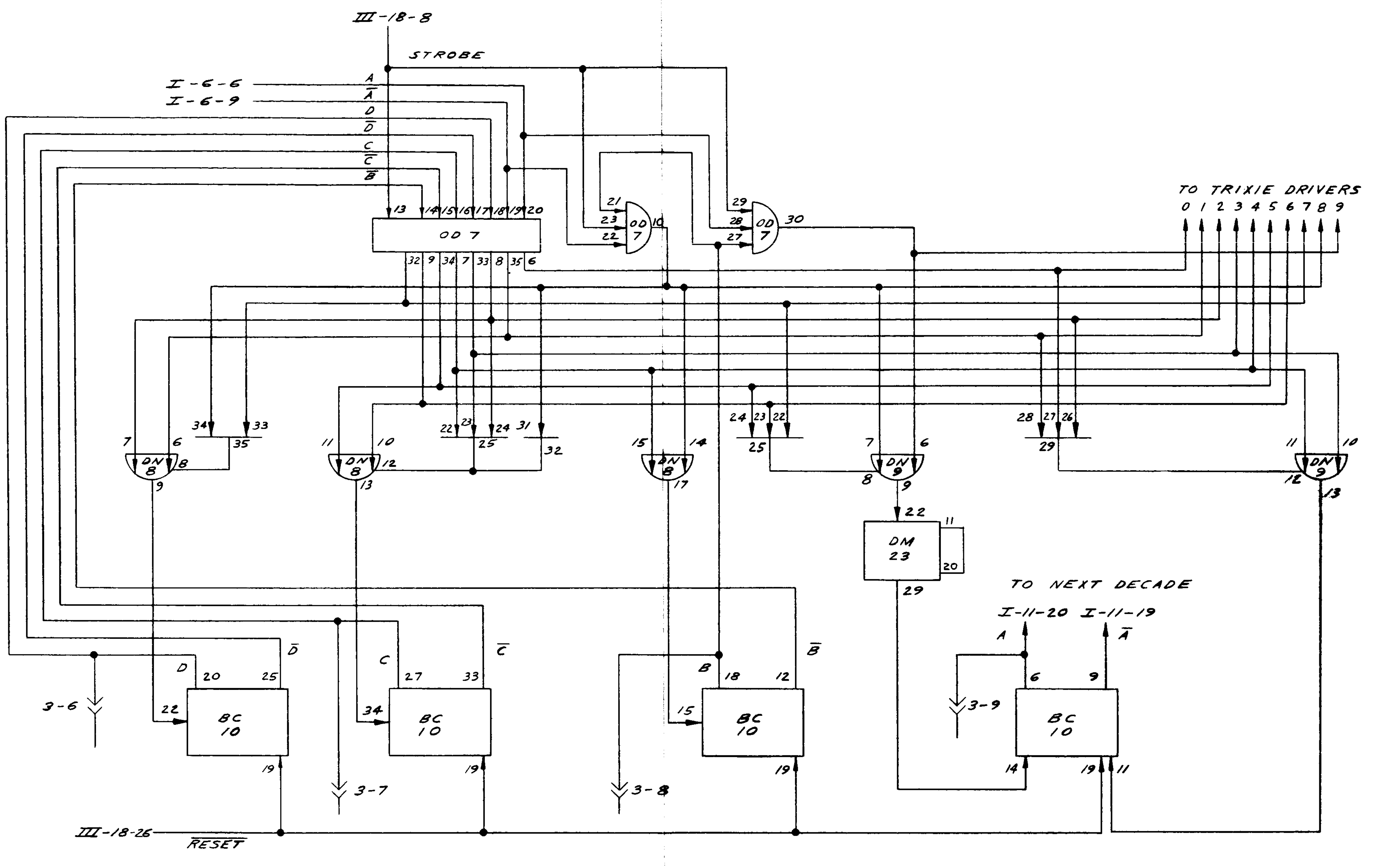
NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.

Figure VI-11. Decimal Display Unit, Binary/BCD Converter 1, Decade 4 (S-Block II)



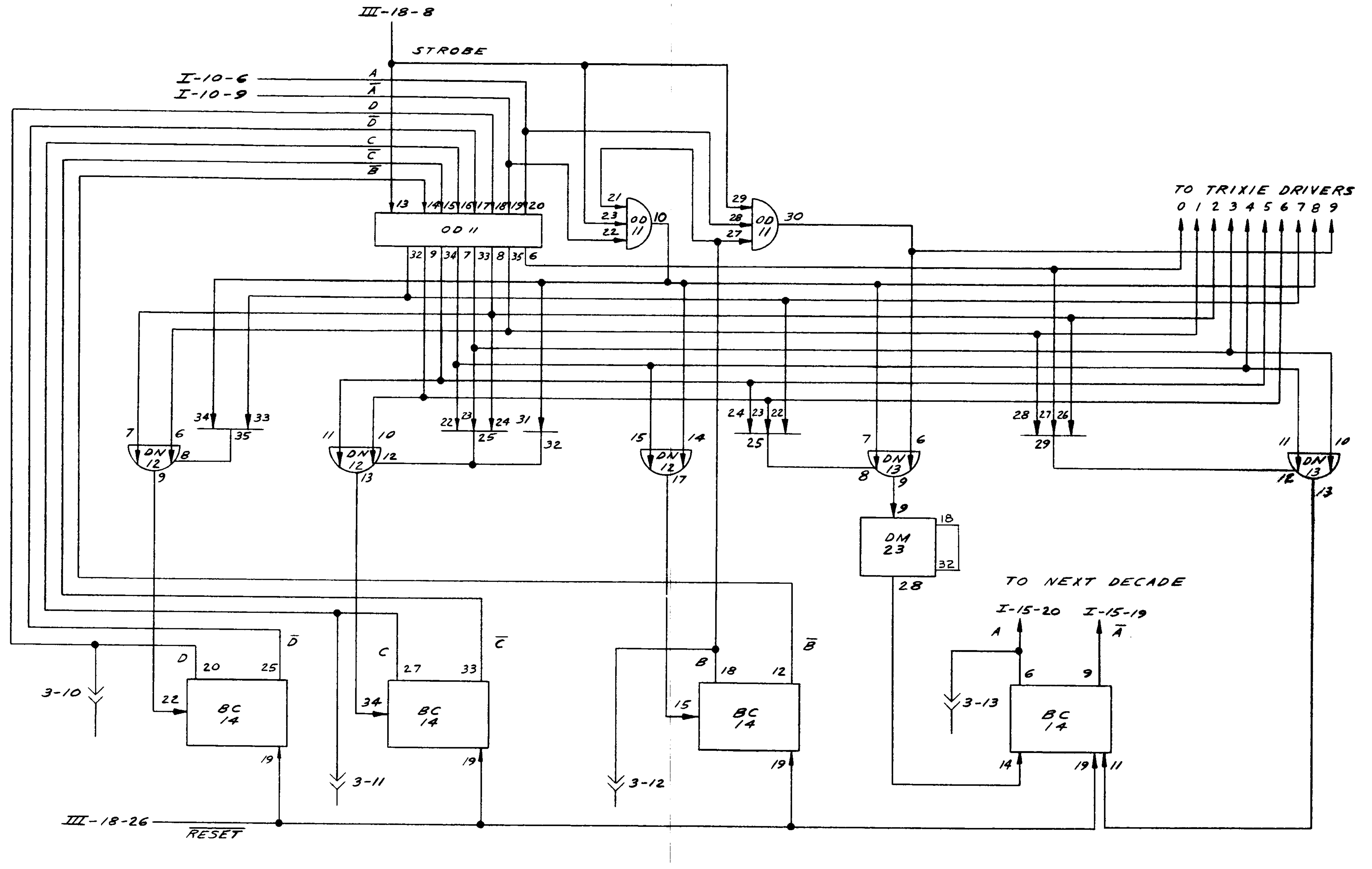
NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.

Figure VI-12. Decimal Display Unit, Binary/BCD Converter 1, Decade 5 (S-Block II)



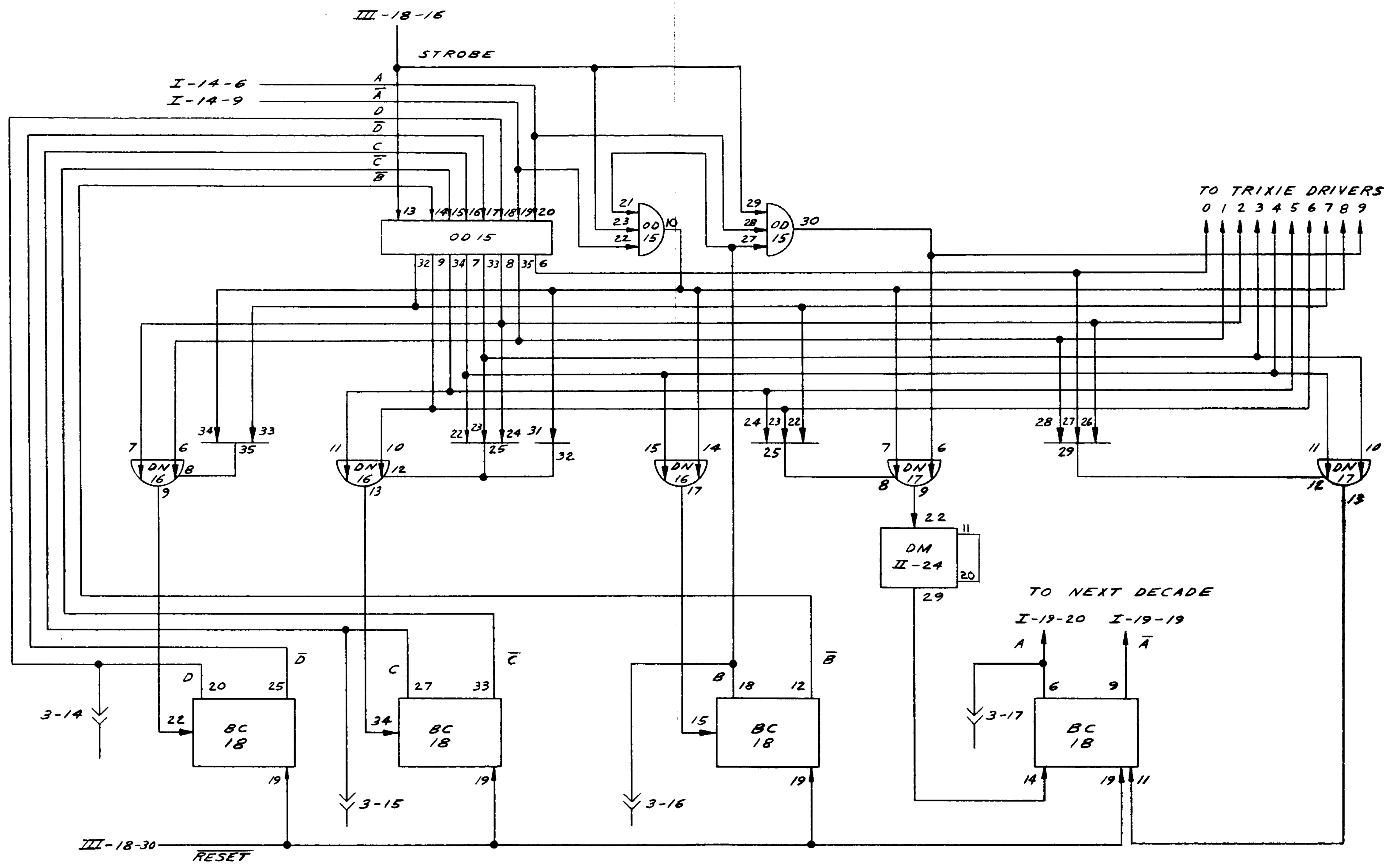
NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.

Figure VI-13. Decimal Display Unit, Binary/BCD Converter 2, Decade 2 (S-Block I)



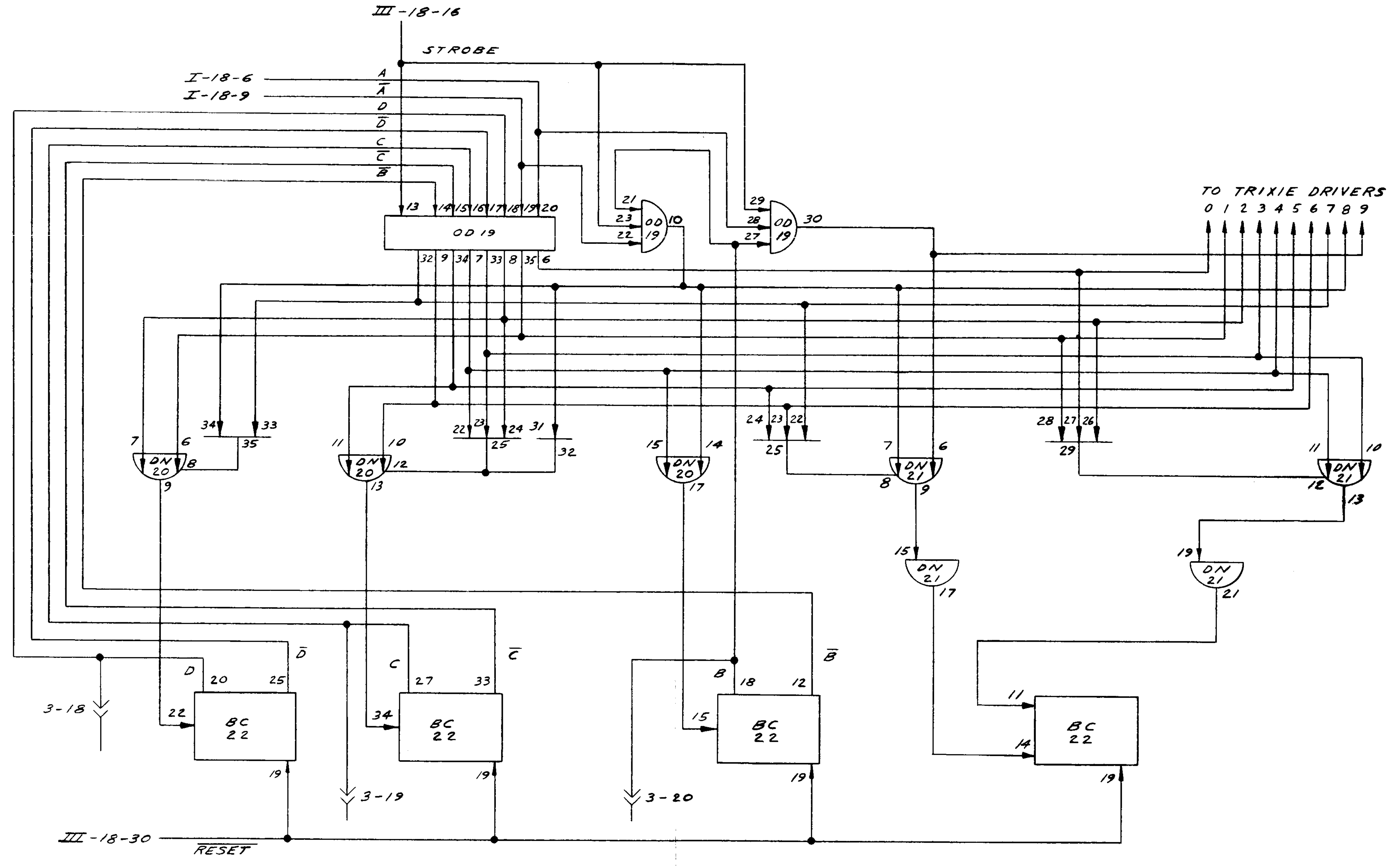
NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.

Figure VI-14. Decimal Display Unit, Binary/BCD Converter 2, Decade 3 (S-Block I)



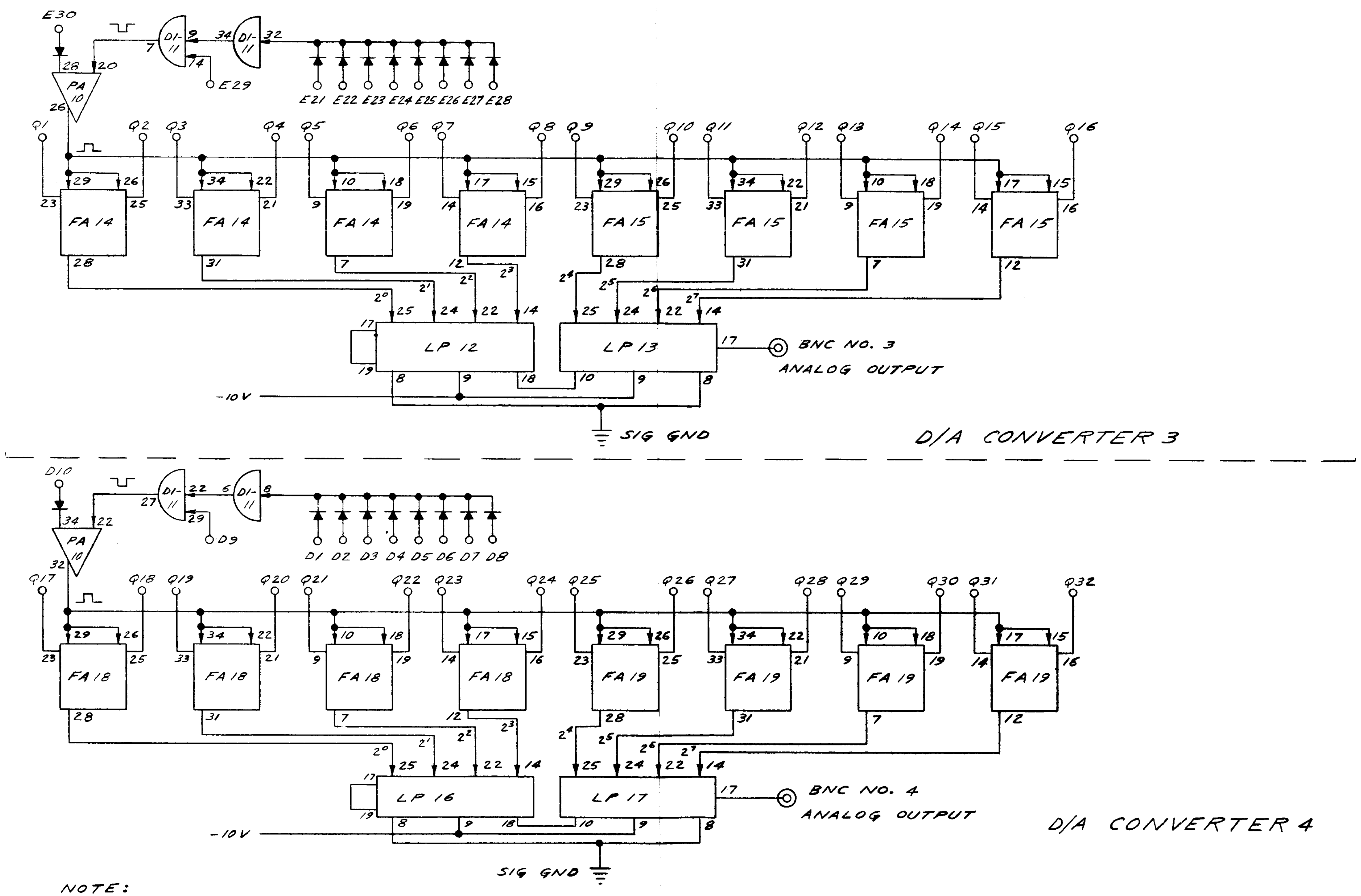
NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.

Figure VI-15. Decimal Display Unit, Binary/BCD Converter 2, Decade 4 (S-Block I)



NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.

Figure VI-16. Decimal Display Unit, Binary/BCD Converter 2, Decade 5 (S-Block I)



NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.
2. ALL DIODES ARE IN277 AND ARE LOCATED ON COMPONENT BOARDS EXTERNAL TO S-BLOCK I.

Figure VI-17. Quick Look Unit, D/A Converter 3 & 4 (S-Block I)

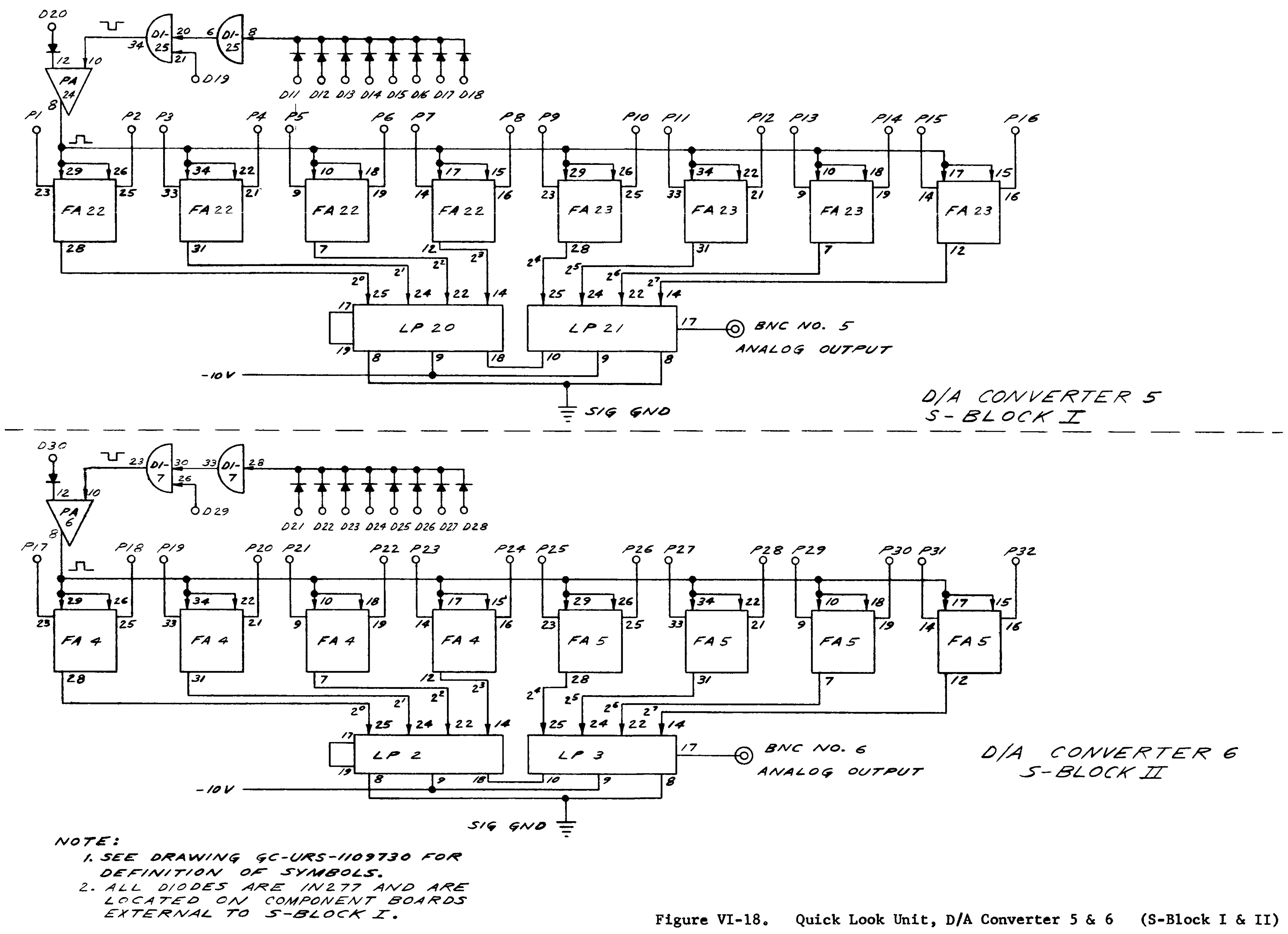
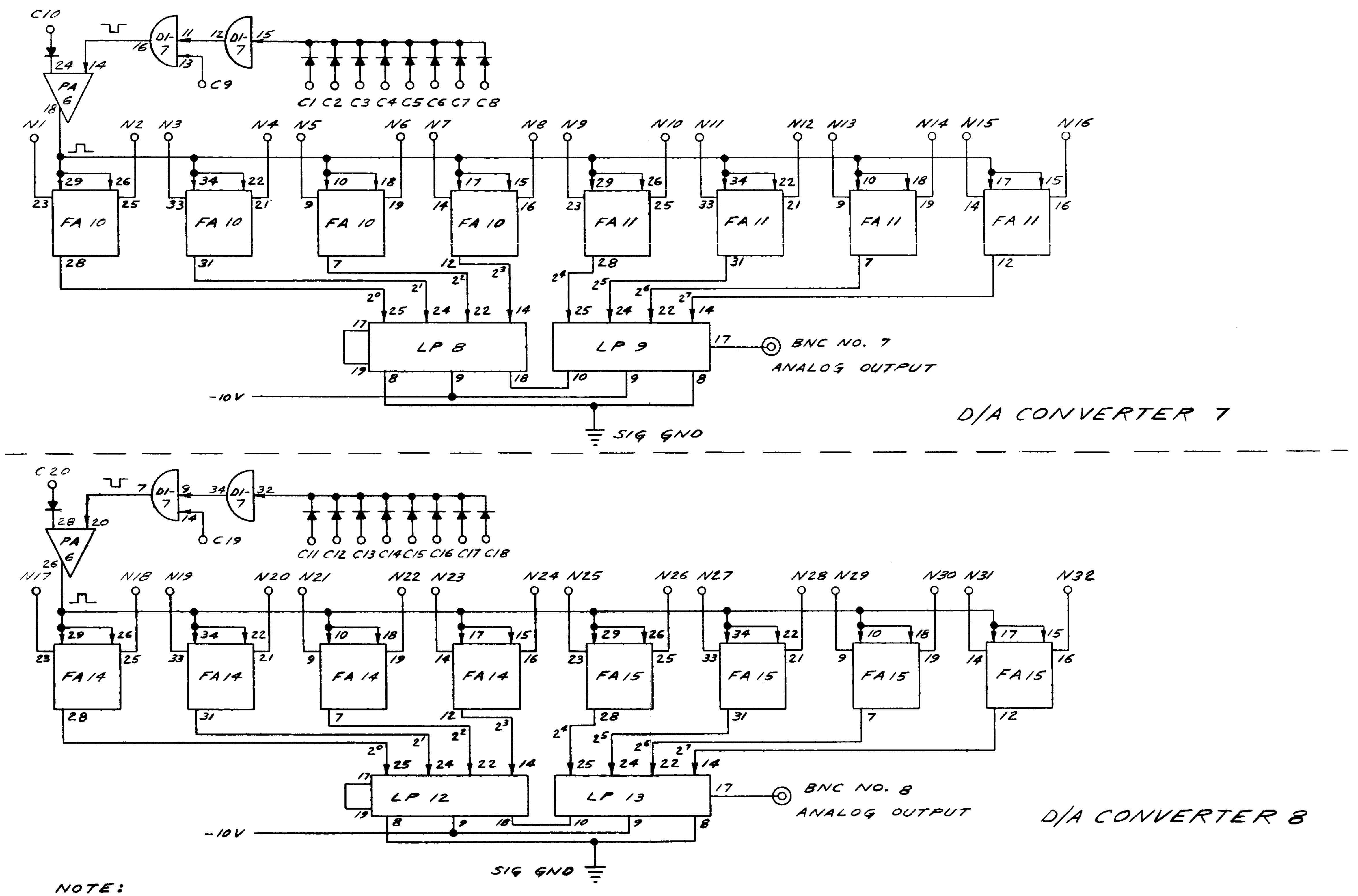


Figure VI-18. Quick Look Unit, D/A Converter 5 & 6 (S-Block I & II)



NOTE:
1. SEE DRAWING GC-URS-1109730 FOR DEFINITION OF SYMBOLS.
2. ALL DIODES ARE IN277 AND ARE LOCATED ON COMPONENT BOARDS EXTERNAL TO S-BLOCK I.

Figure VI-19. Quick Look Unit, D/A Converter 7 & 8 (S-Block II)

N64-29189

ERRATA

Page IV-29 -- Add as follows in columns "From" & "To", respectively: E8 to K8, E10 to K10, E12 to K12, E14 to K14, and E16 to K16.

Page IV-32 -- Columns "From" & "To", respectively, add C25 to C31; and change "C31" to "C32", "C32" to "C33" in the "To" column.

Page IV-33 -- "To" column, change "V16" to "T14 and E34"; and in "Signals" column delete "EWL".

Page IV-34 -- "To" column, change "A12" to "A16".